

COMPAL CONFIDENTIAL

MODEL NAME : *Biathlon (IBM 15R)*
COMPAL P/N : *HEL00*
PCB NO : *LA-3091P*
Revision : *1.0*

IBM 15R Schematics Document
uFCBGA/uFCPGA Mobile Dothan
Alviso 915+ ICH6-M
2 Channel DDR2

2005-12-20
REV : 1.0

SW LED/B
LS-3093P

M/B LA-3091P

TP/B
LS-3094F

LED/B
LS-3092P

Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Bithlon LA3091 Schematic	
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				Custom	LA-3091
				Date	Tuesday, January 10, 2006
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				Rev	1.0



Security Classification	Compal Secret Data			Custom		
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	Functional Block	
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I2C / SMBUS ADDRESSING

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	F
CARD BUS	AD20	1	A
Cardreader			B
1394	AD16	2	E
Wireless LAN(MINI PCI)	AD18	3	G,H

@ Depop
1@ IBM 15R (UMA)
2@ (Discrete)

Power Managment table

Signal State	+12VALW +5VALW +3VALW	+12V +5V +3V +1.8V	+CPU_CORE +VCCP +5VS +3VS +2.5VS +1.8VS +1.25VS +1.5VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

Ceramic Capacitor Spec
Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	COG		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1PF	+2%	+3%	+5%

K	M	N	P	Q	V	X	Z	
+10%	+20%	+30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

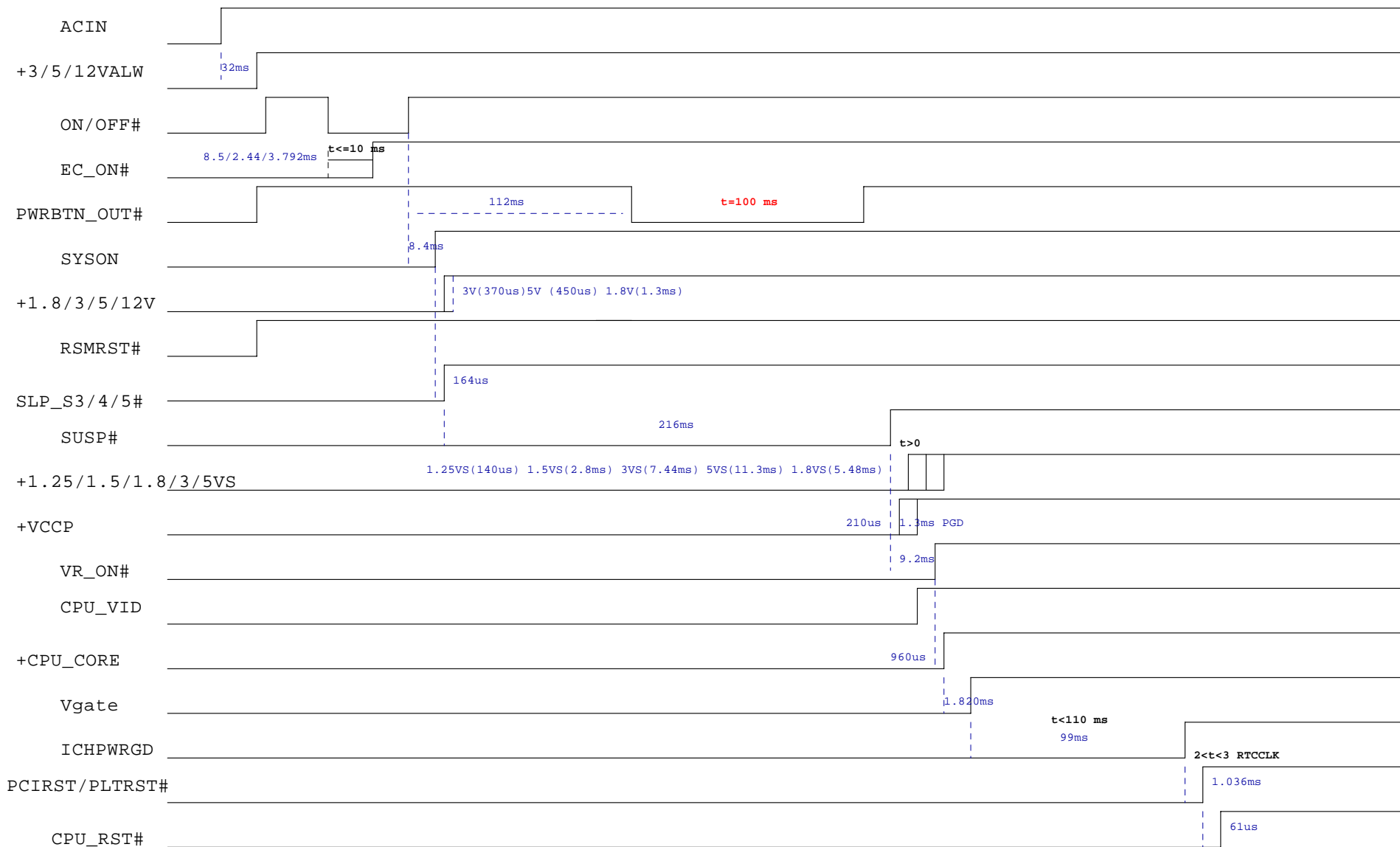
SMBUS Control Table

	SOURCE	BATT	SERIAL EEPROM	THERMAL SENSOR CPU (ADM1032)	Intel PCI WLAN	SO-DIMM1 SO-DIMM2	CLK CHIP	LCD
SMB_EC_CK1 SMB_EC_DA1	KB910L PU +5VALW	✓	✓					
SMB_EC_CK2 SMB_EC_DA2	KB910L PU +5VALW			✓	✓			
ICH_SMBCLK ICH_SMBDATA	ICH6-M PU +3VALW					✓	✓ PU +3VS	
LCD_CLK LCD_DAT	Alviso GM-GP PU +2.5VS							✓ PU +3VS

	PCB Rev	Data
EVT-Build	0.1	
DVT-Build	0.2	
PVT-Build		
MP-Build		

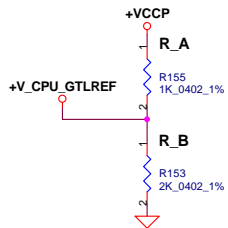
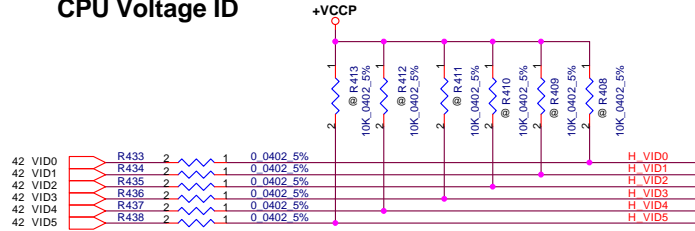
SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK
0.1		EVT-Build
0.2		DVT-Build
		PVT-Build
		MP-Build



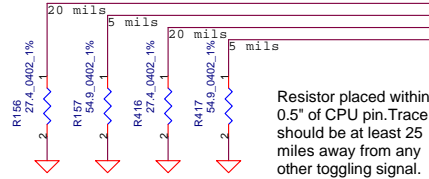
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CPU Voltage ID

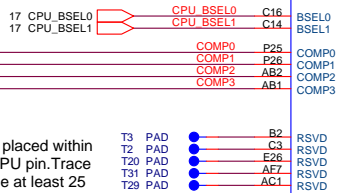
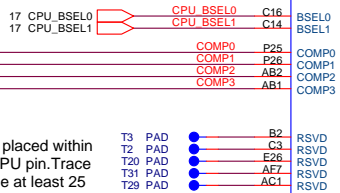
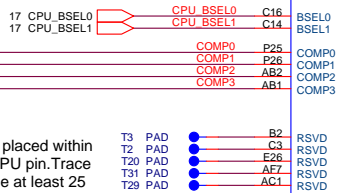
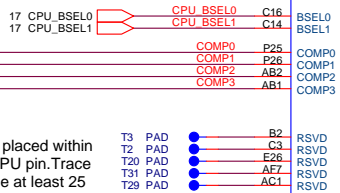
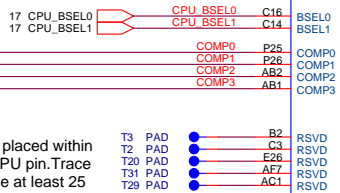
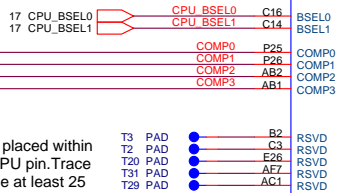
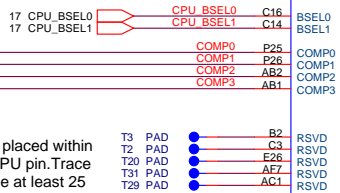
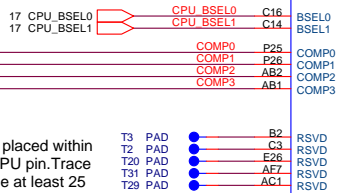
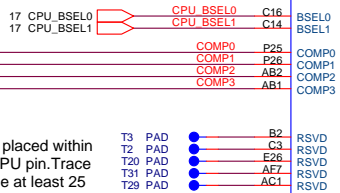
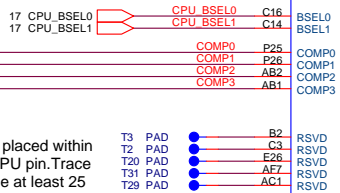
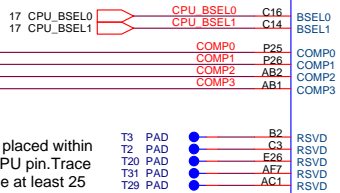
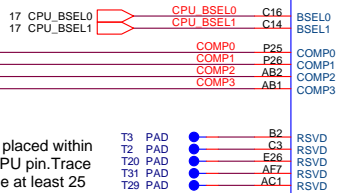
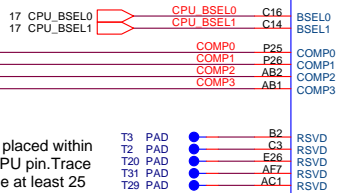
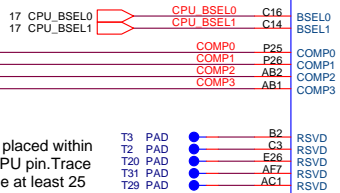
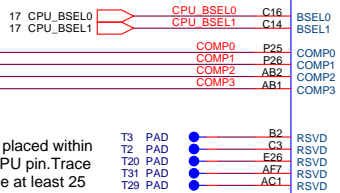
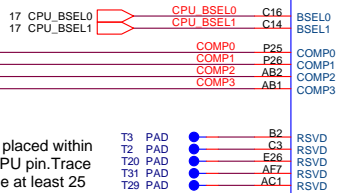
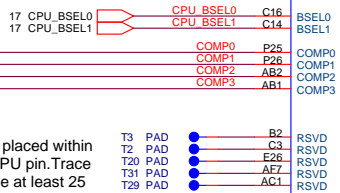
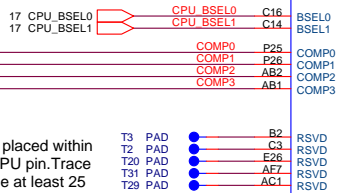
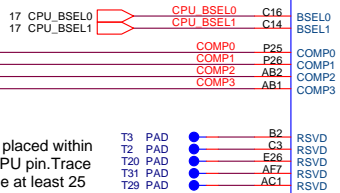
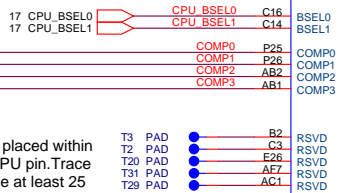
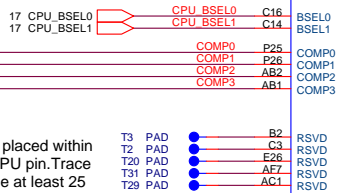
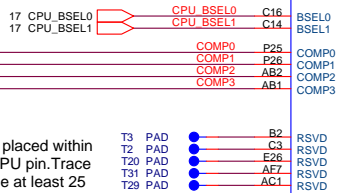
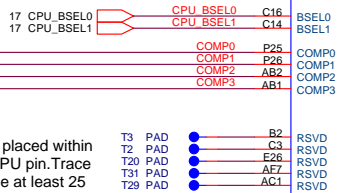
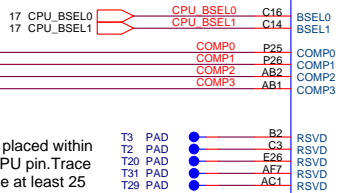
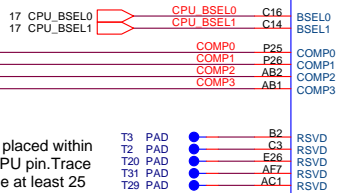
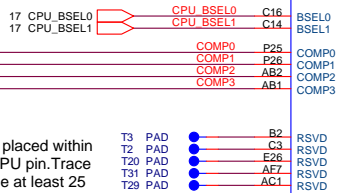
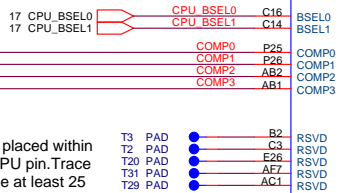
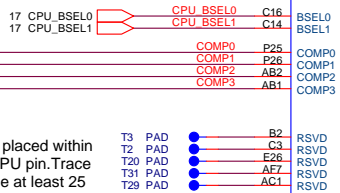
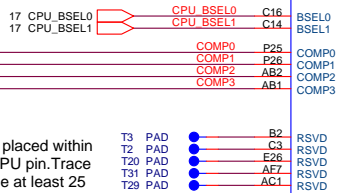
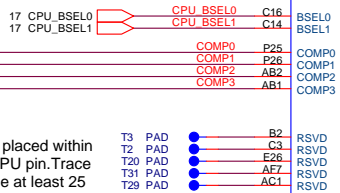
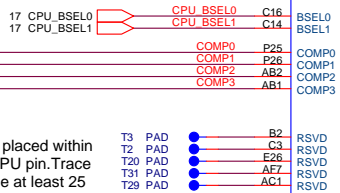
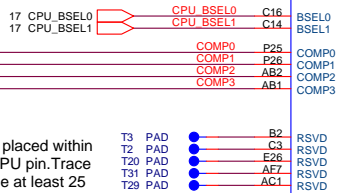
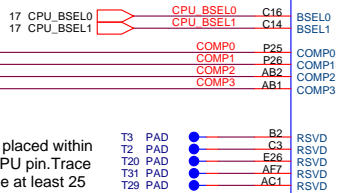
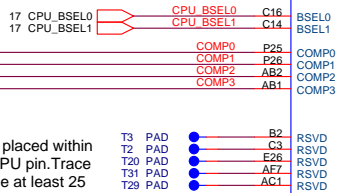
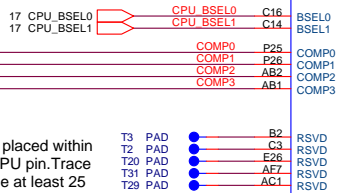
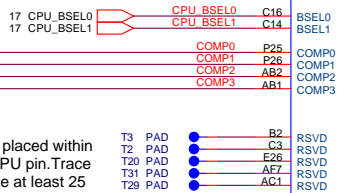
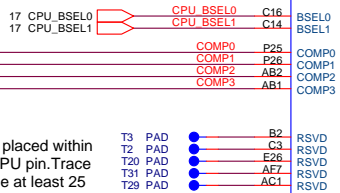
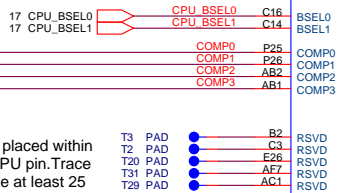
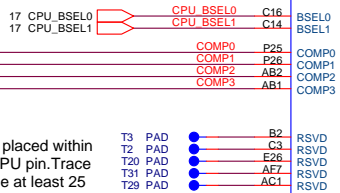
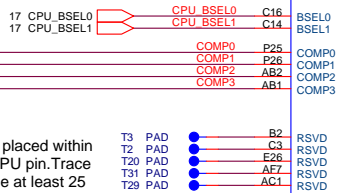
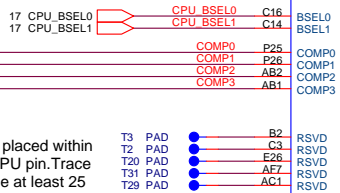
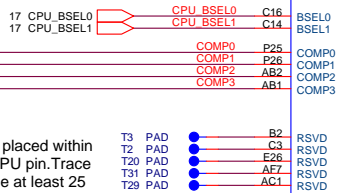
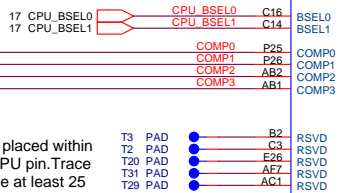
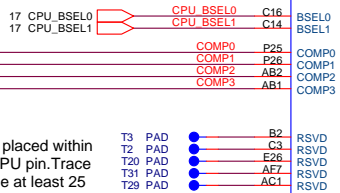
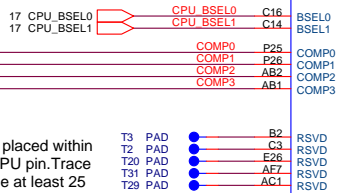
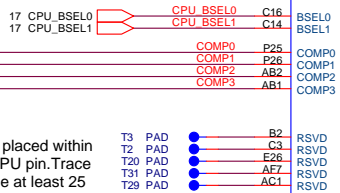
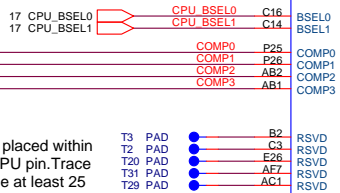
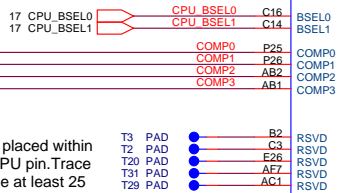
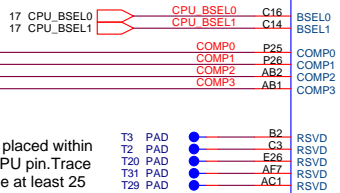
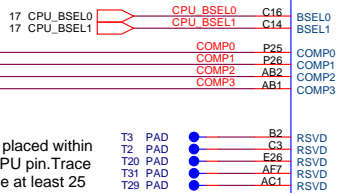
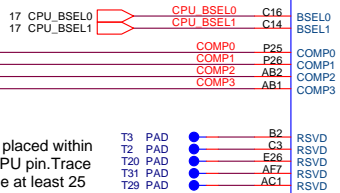
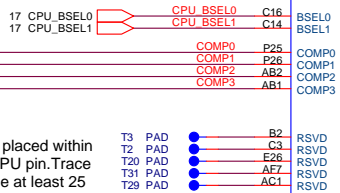
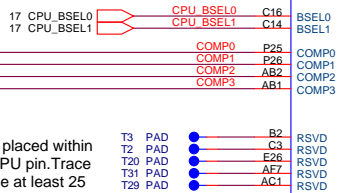
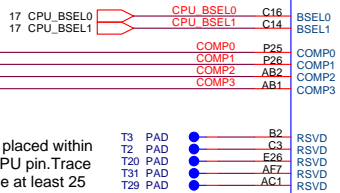
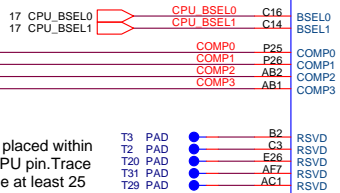
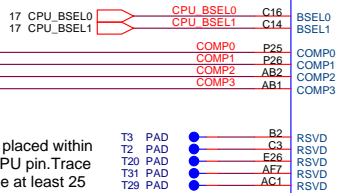
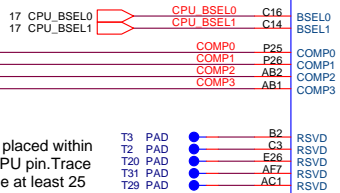
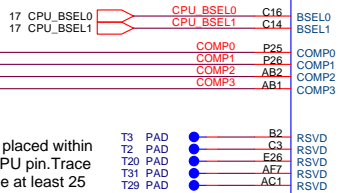
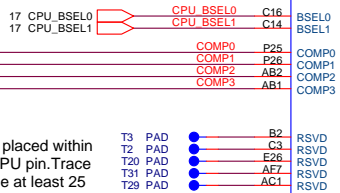
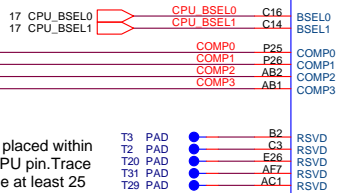
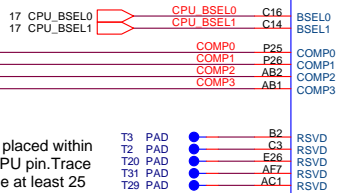
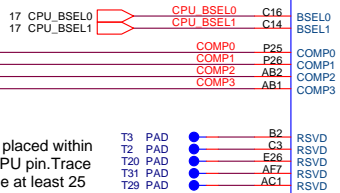
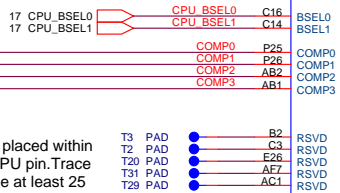
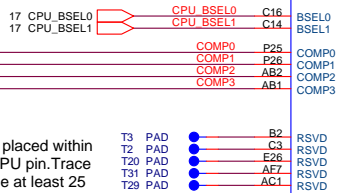
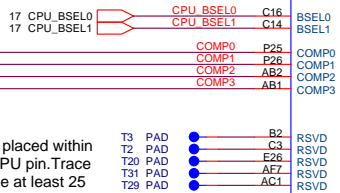
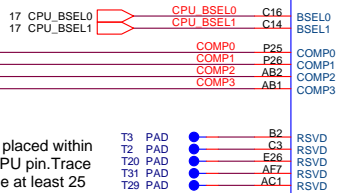
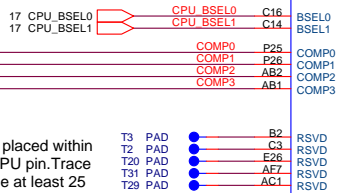
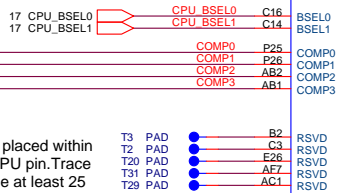
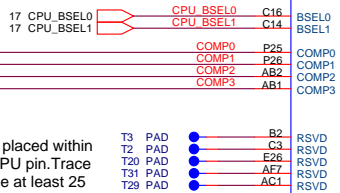


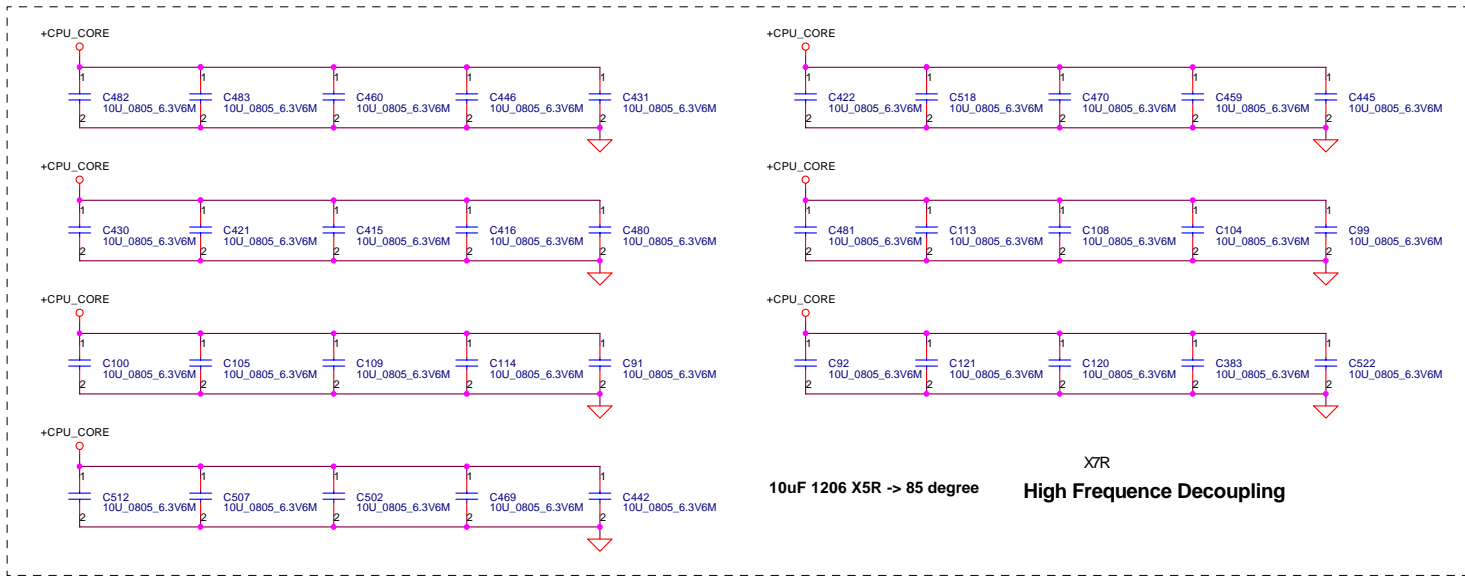
Layout close CPU

Layout Note:
500 mil max length

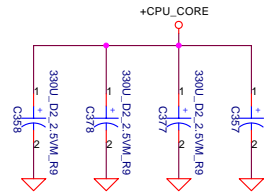


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



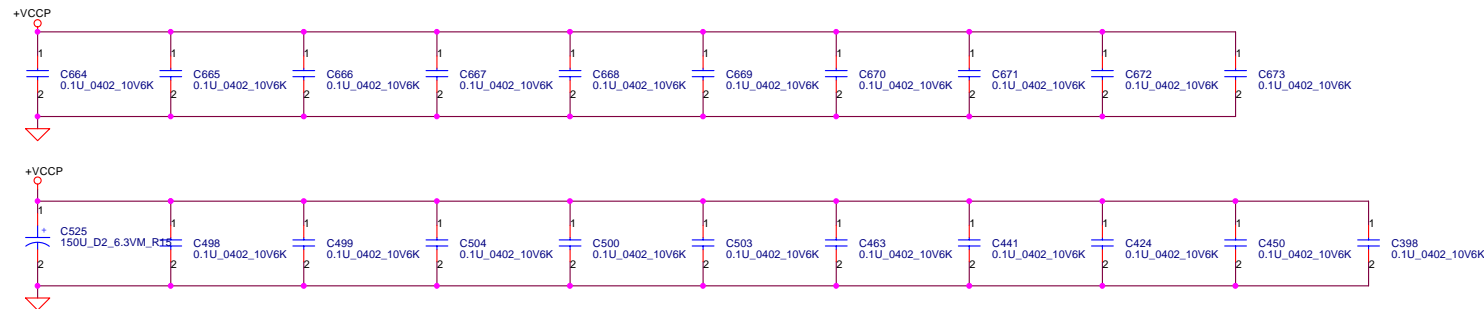


Near VCORE regulator.



ESR <= 3m ohm
Capacitor > 880 uF

Vcc-core Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	3X330uF	9m ohm/3	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

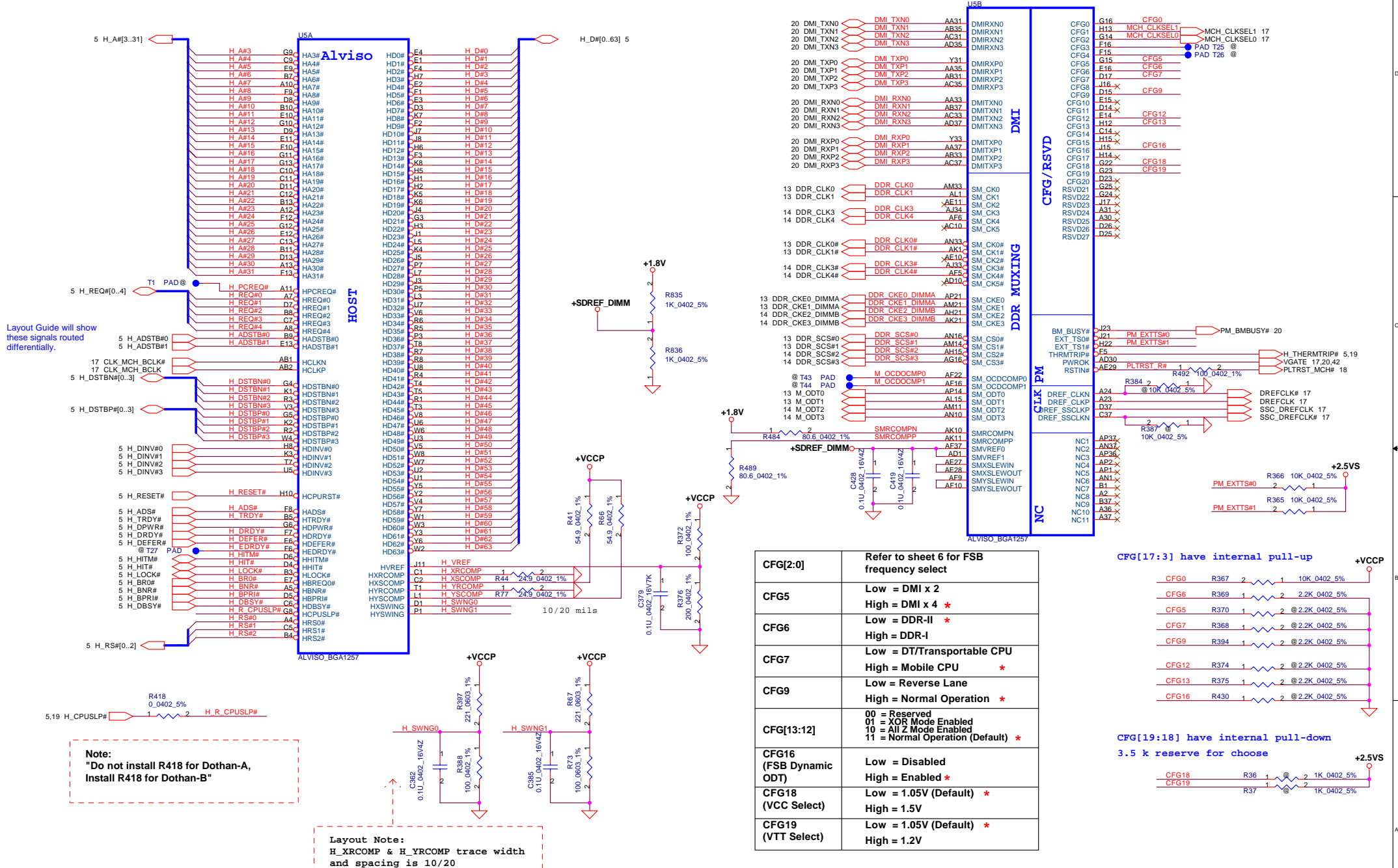


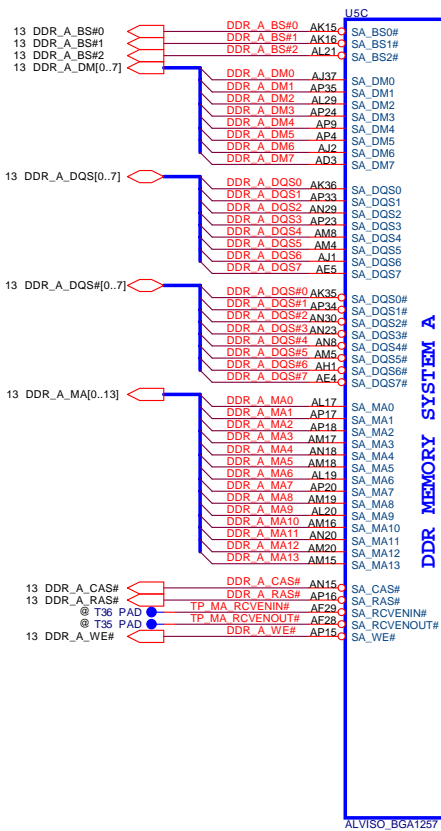
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title
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Date: Tuesday, January 10, 2006				Size Document Number LA-3091 Rev 1.0
Sheet 7 of 44				

Layout Guide will show these signals routed differentially.

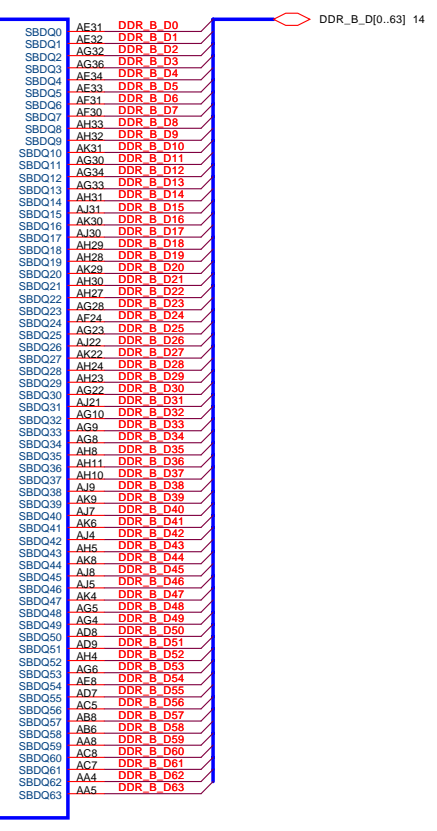
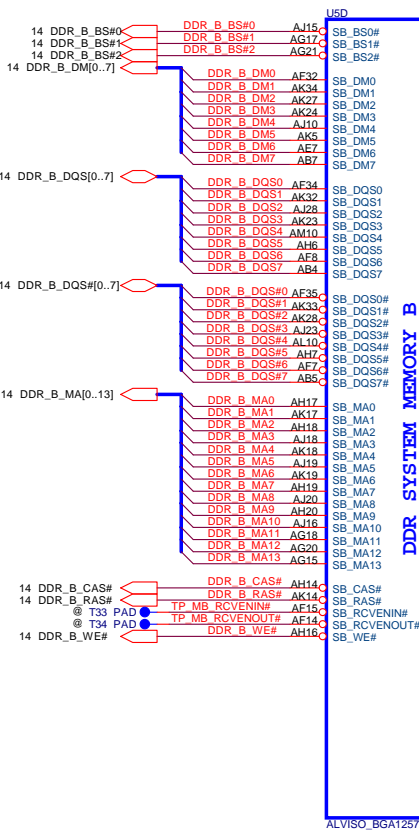
Layout Guide will show these signals routed differentially.

Alviso CFG[17:3] has internal pull-up

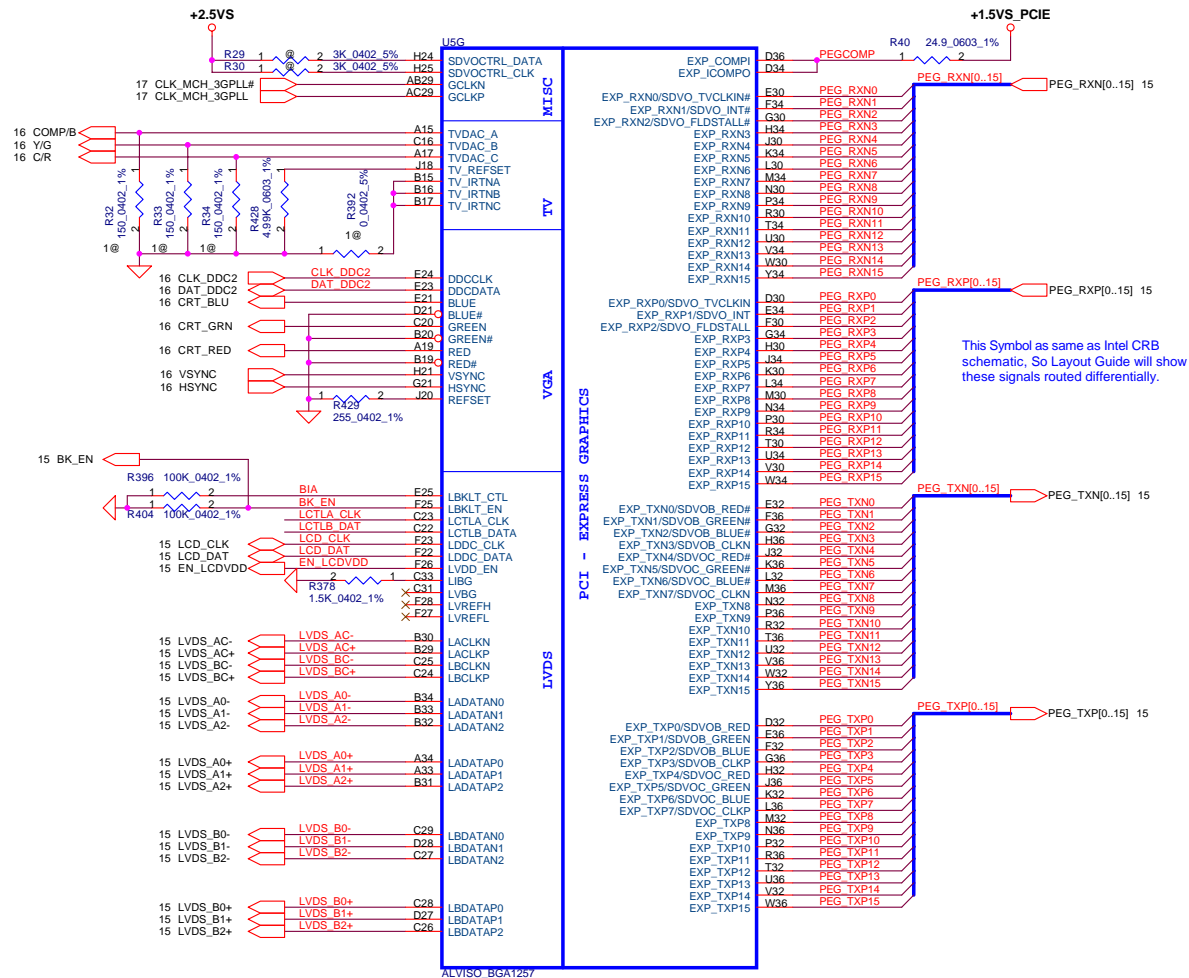




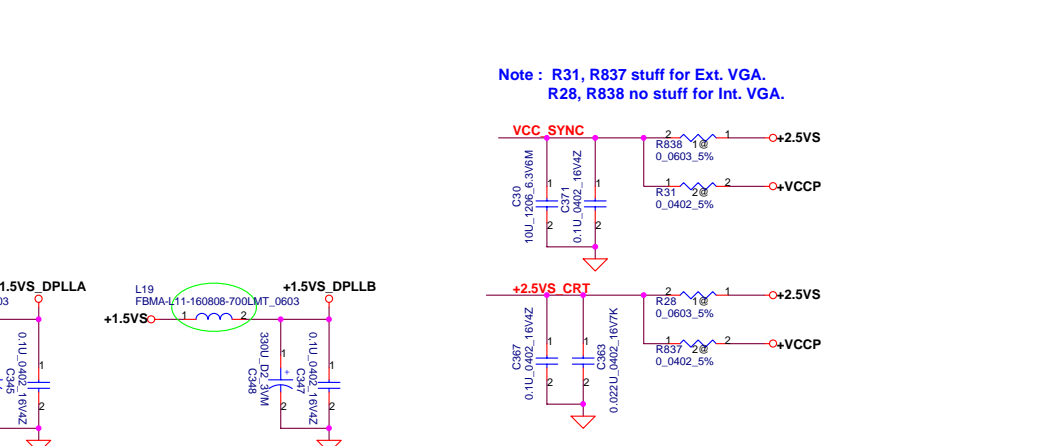
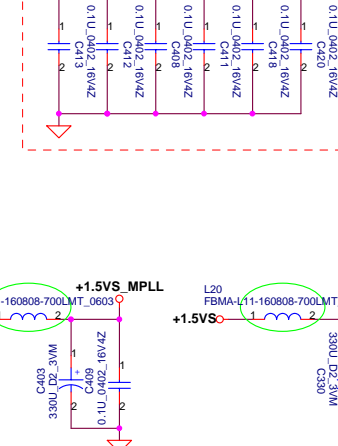
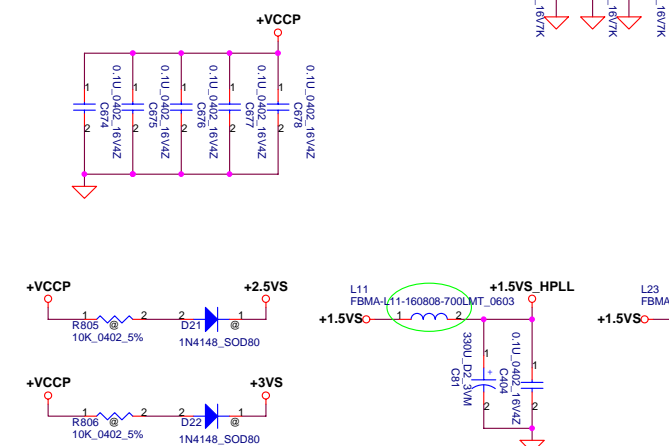
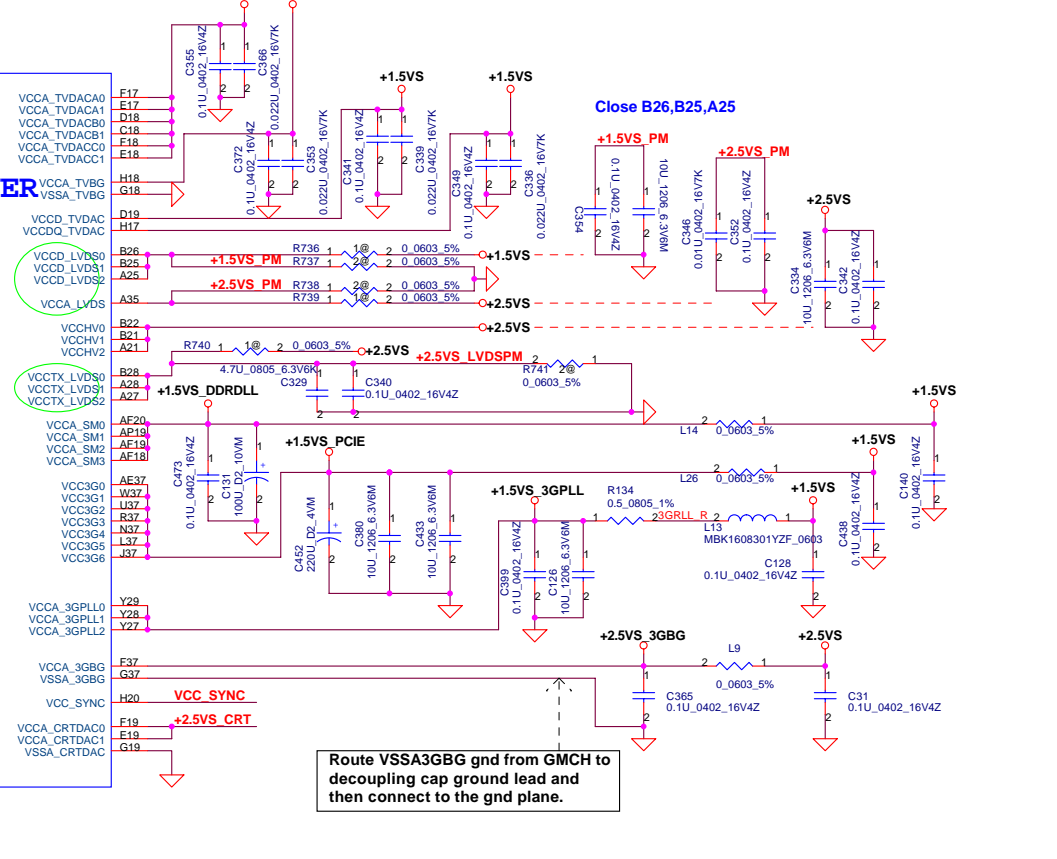
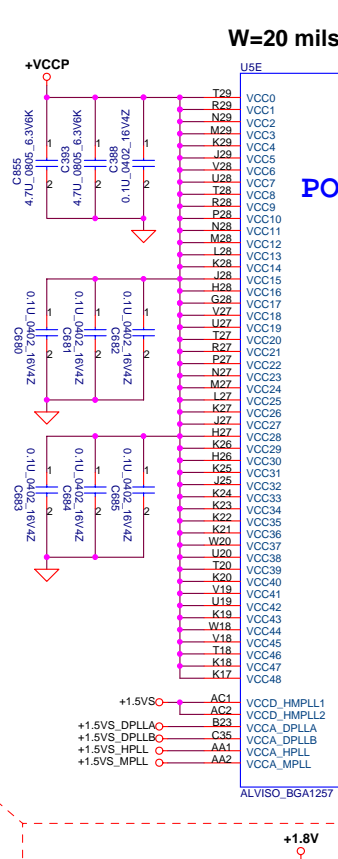
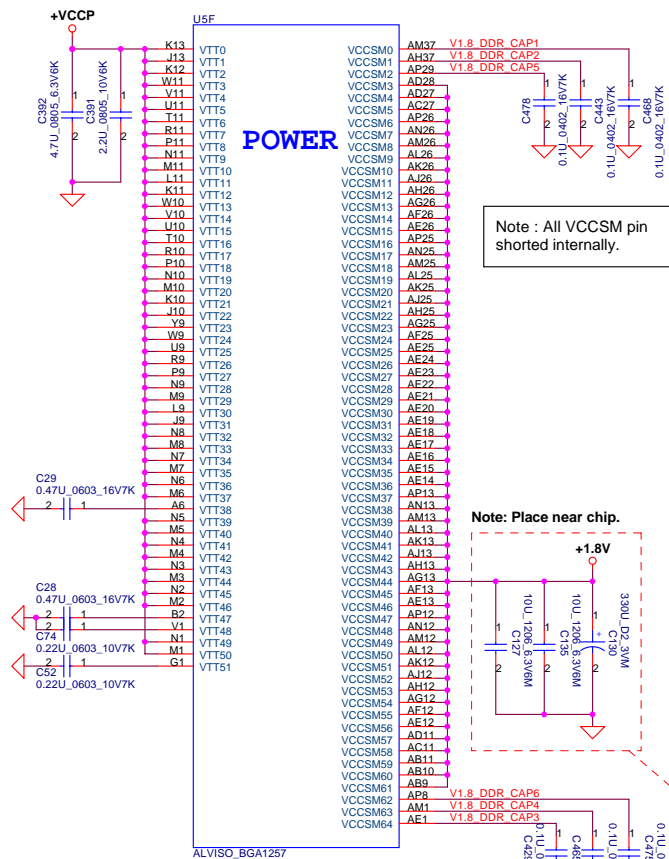
This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



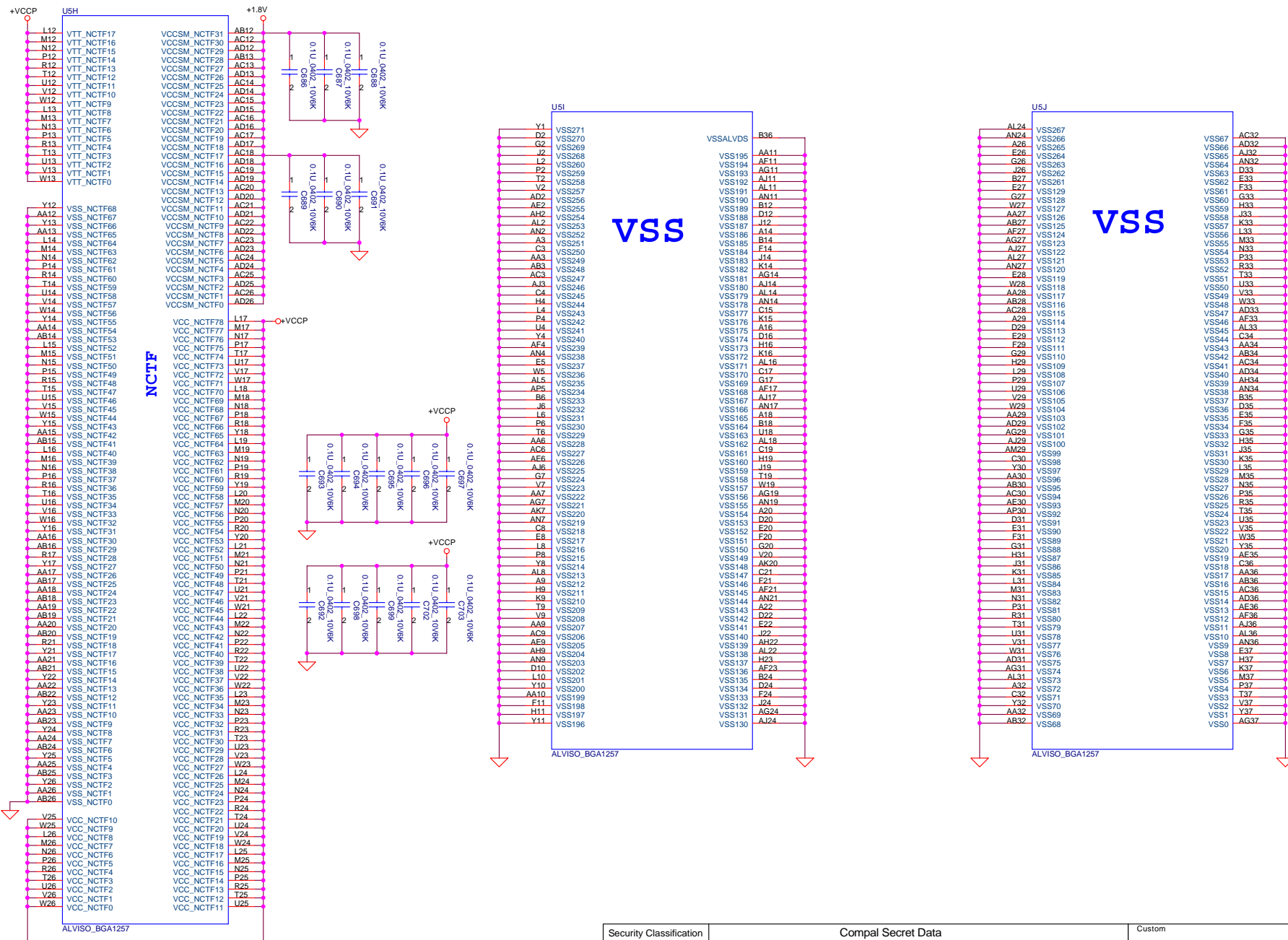
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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	Alviso(2/5)-DDR A/B
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		Date	Tuesday, January 10, 2006	Sheet	10 of 44

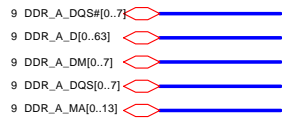


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Size		Document Number		Rev	
LA-3091		1.0		Date	
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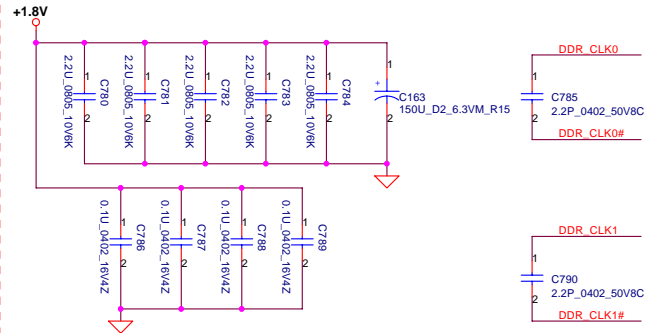


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						Size		Document Number	
		LA-3091				1.0			
3		1		2		Date: Tuesday, January 10, 2006		Sheet 12 of 44	

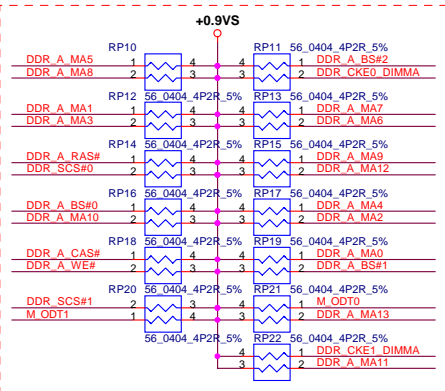
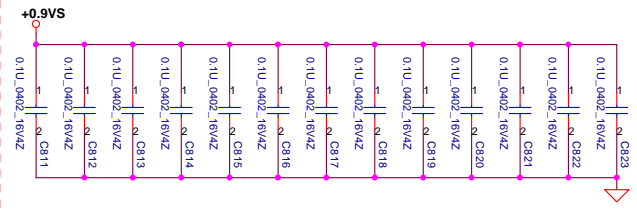
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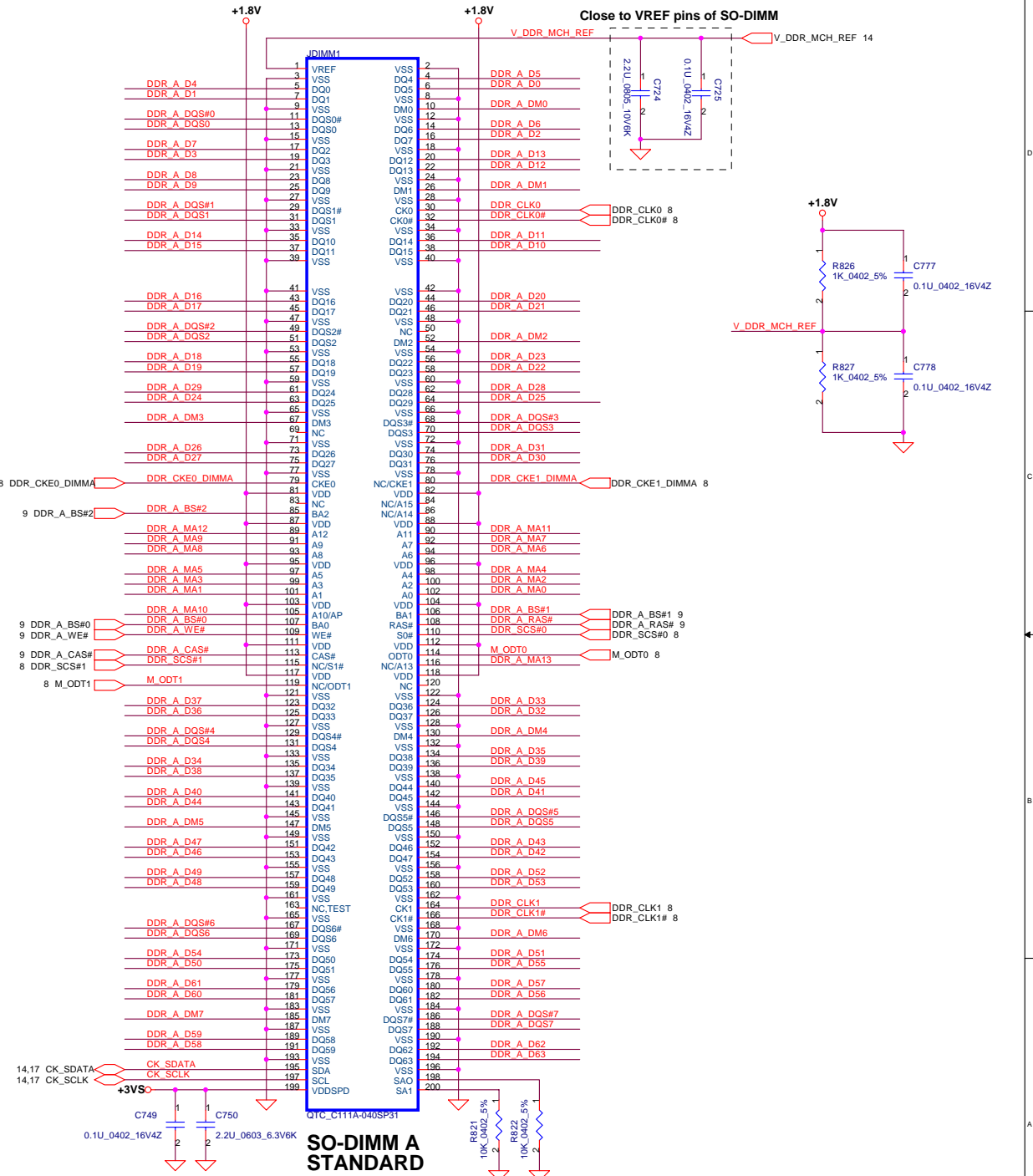
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



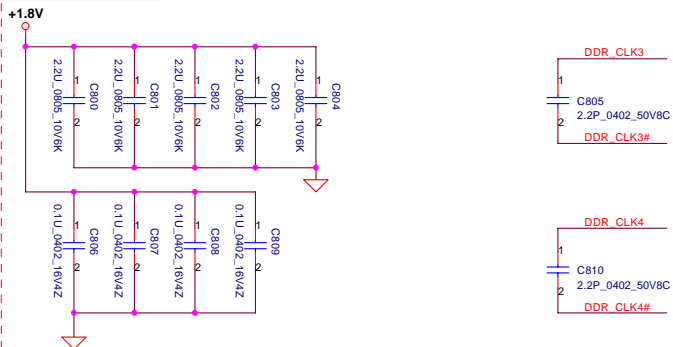
Layout Note:
Place these resistor closely JDIM1, all trace length Max=1.5"



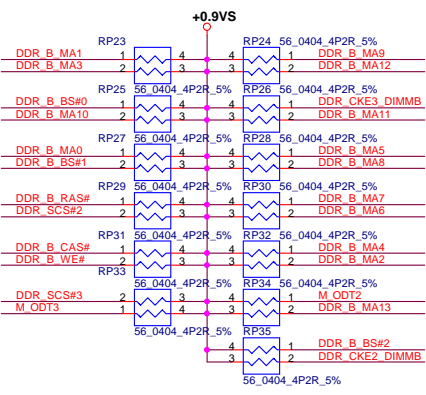
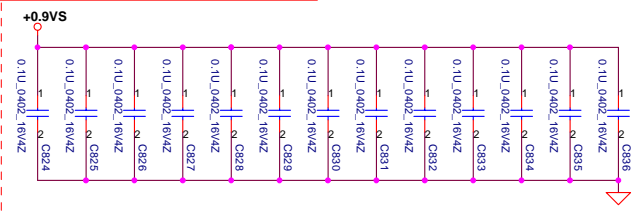
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Size	Document Number	Rev	
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9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS[0..7]
9 DDR_B_MA[0..13]

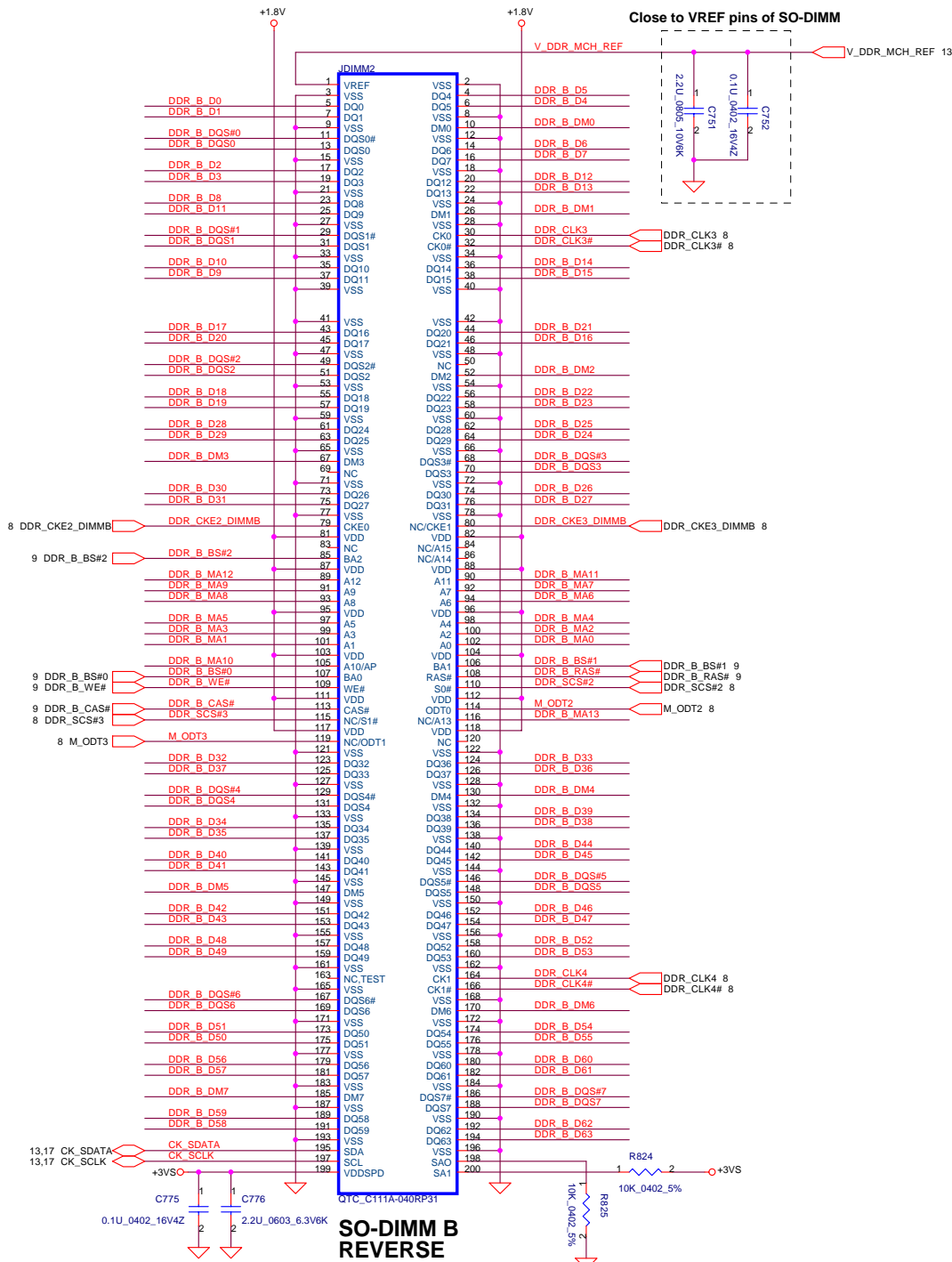
Layout Note:
Place near JDIMM2



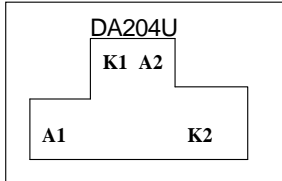
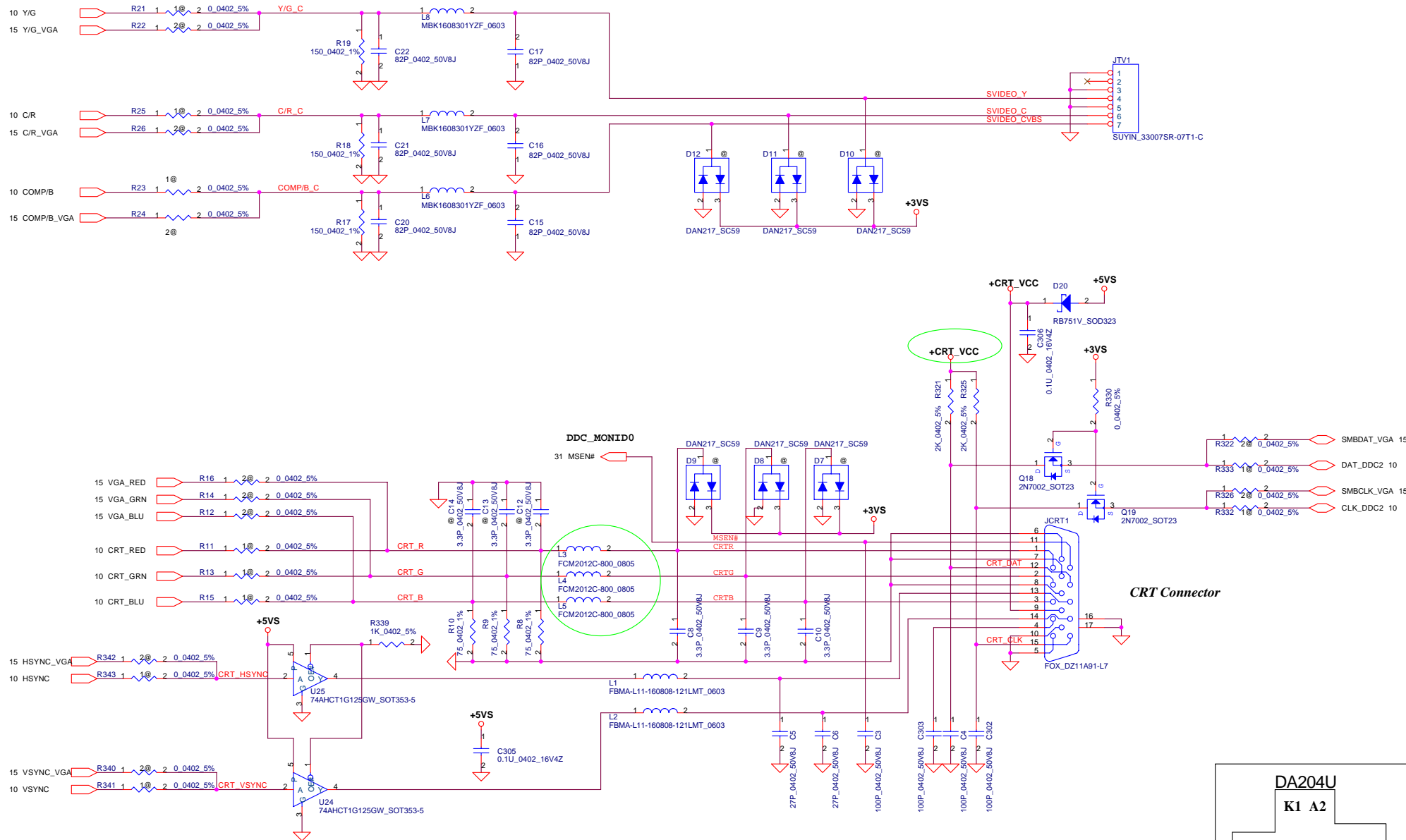
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



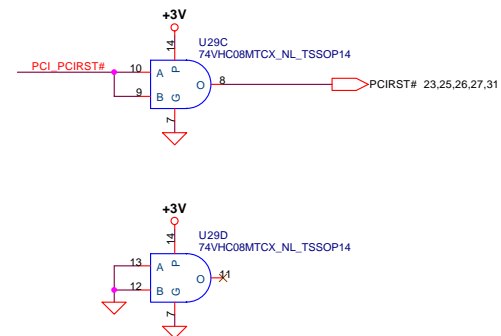
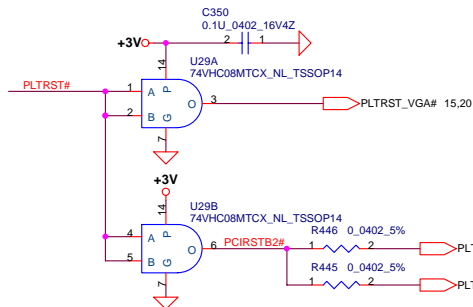
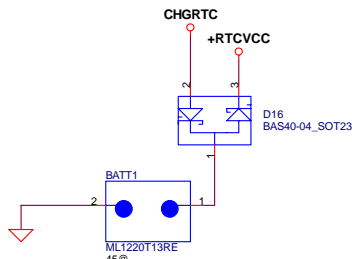
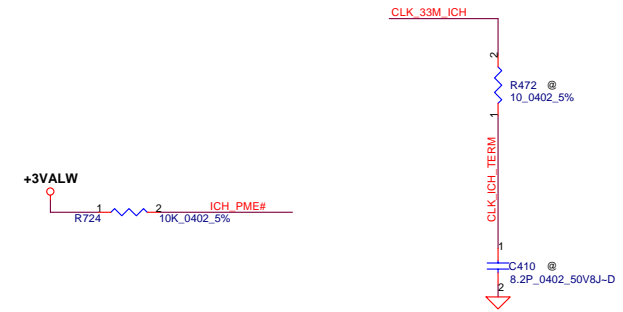
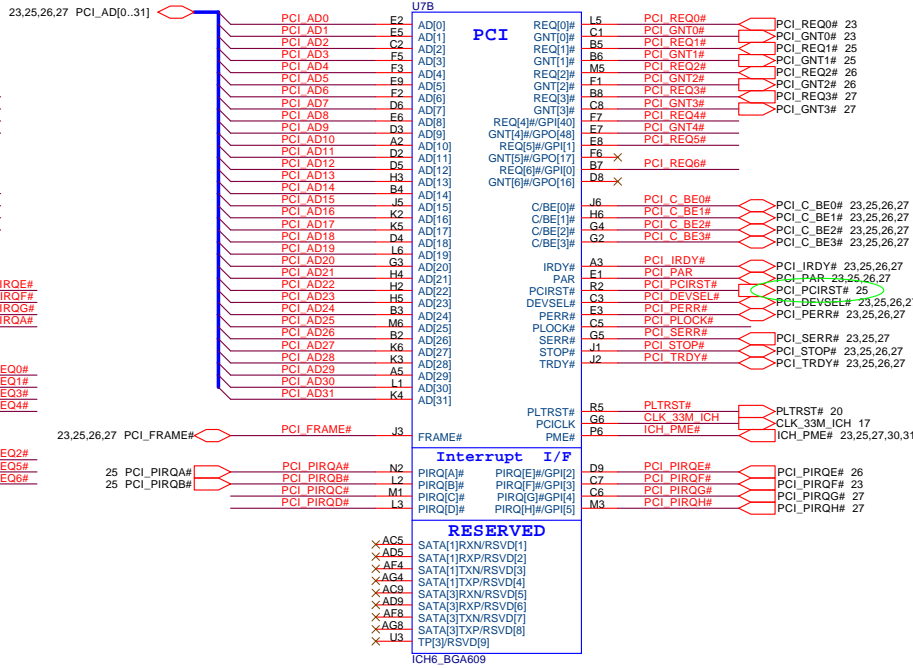
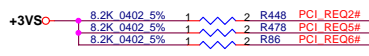
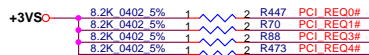
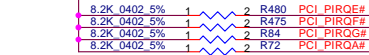
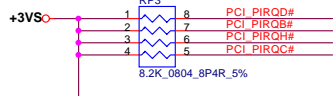
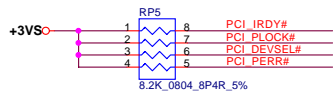
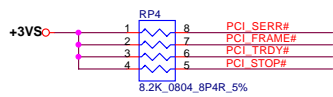
Layout Note:
Place these resistor closely JDIMM2, all trace length Max=1.5"



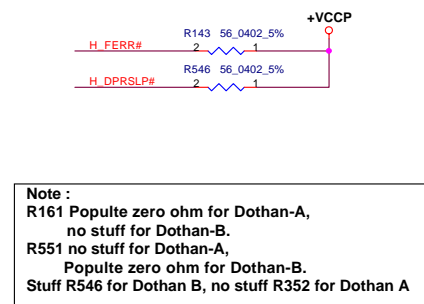
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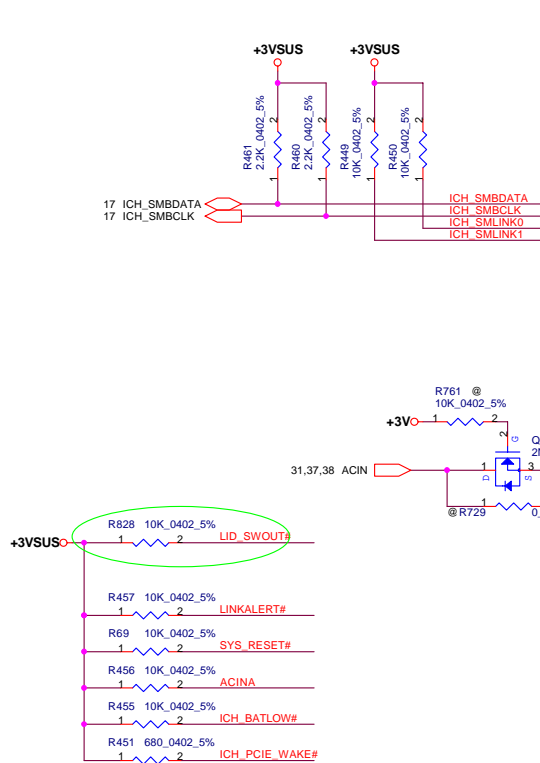
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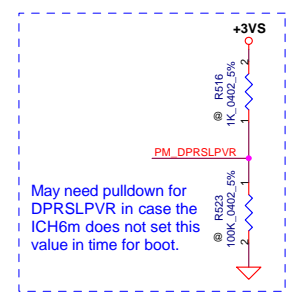
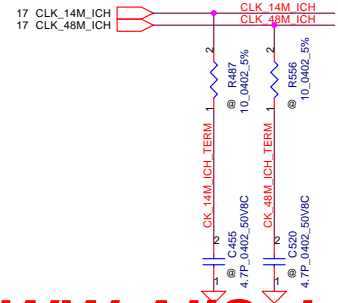
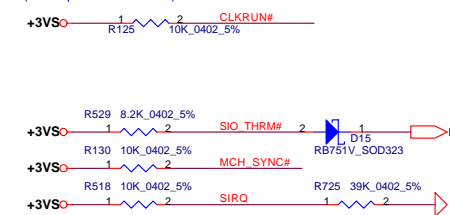
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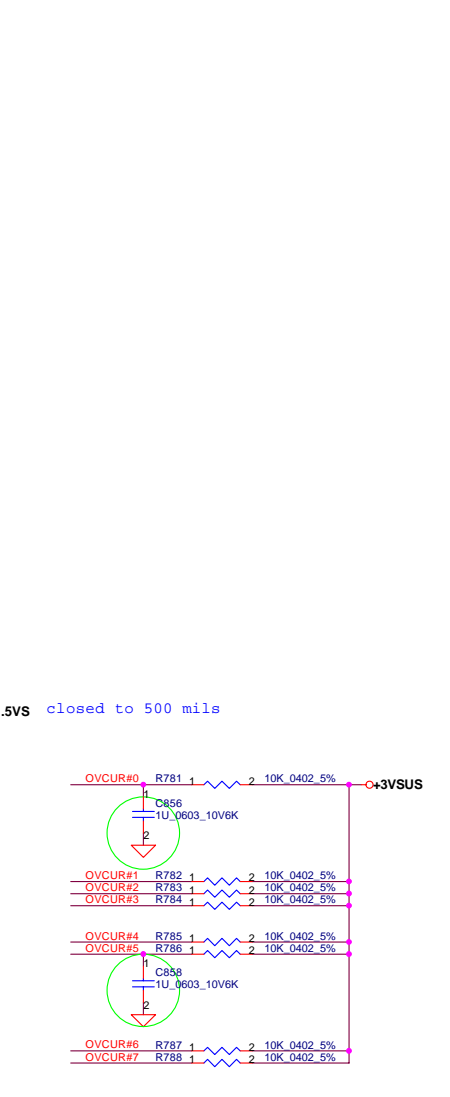
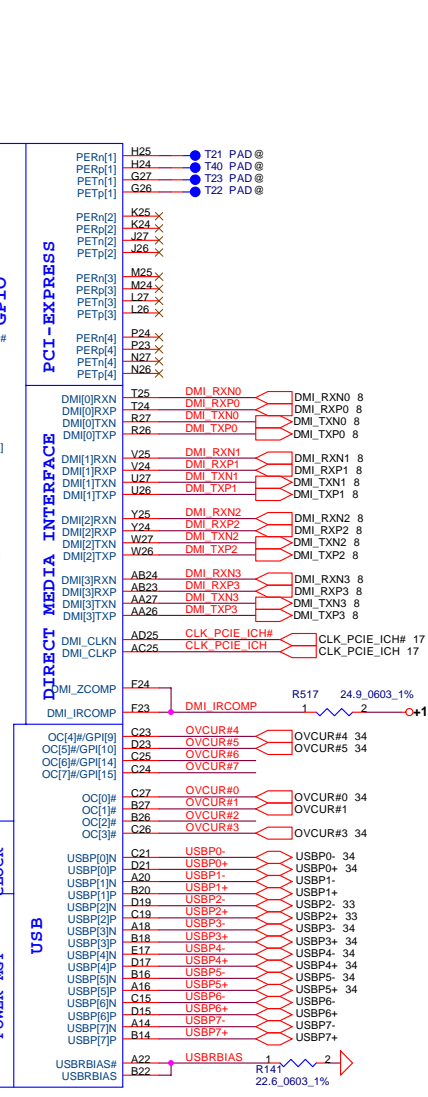
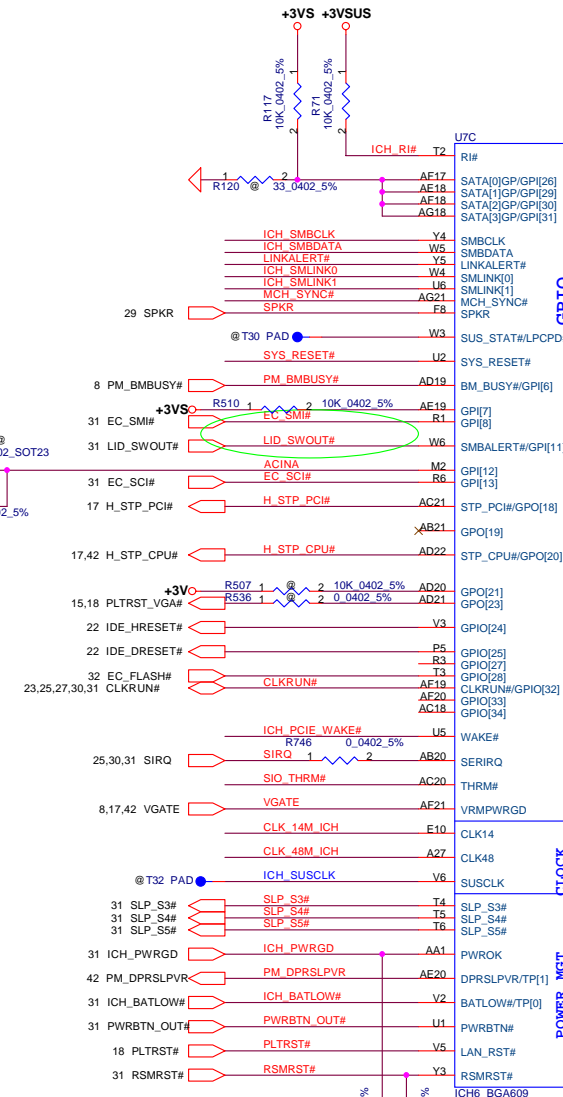
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(PCI Express Wake Event)



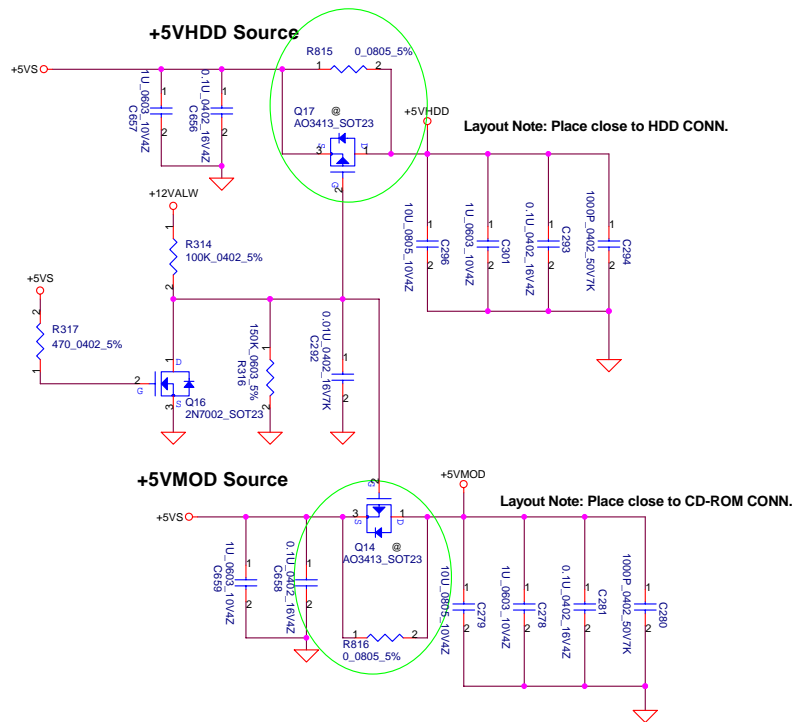
May need pulldown for DPRSLPVR in case the ICH6m does not set this value in time for boot.



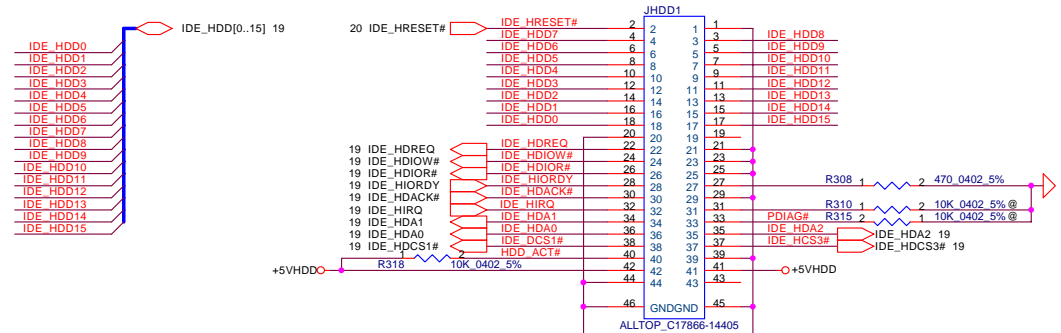
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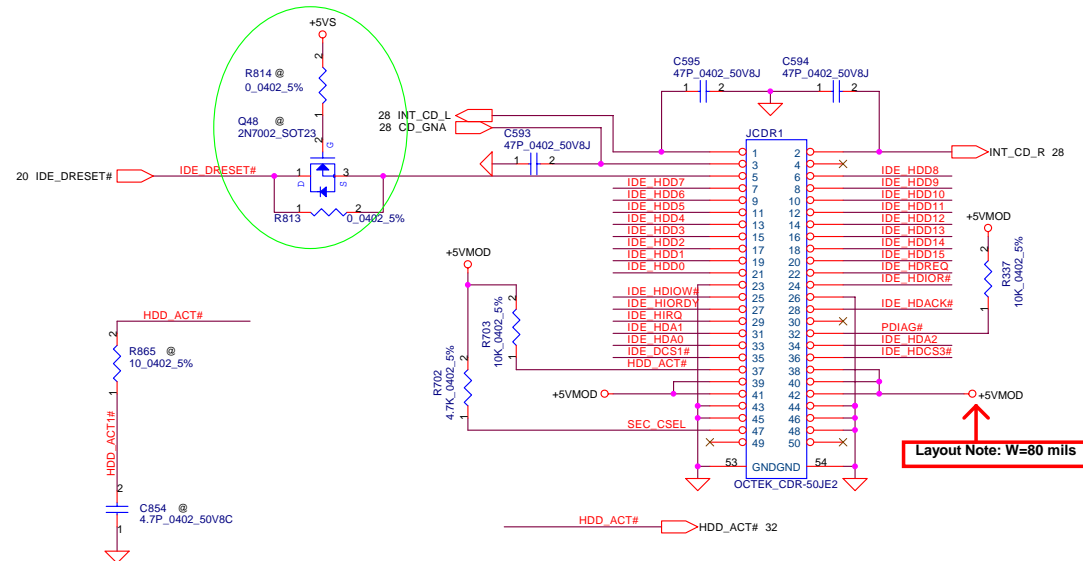


HDD Connector



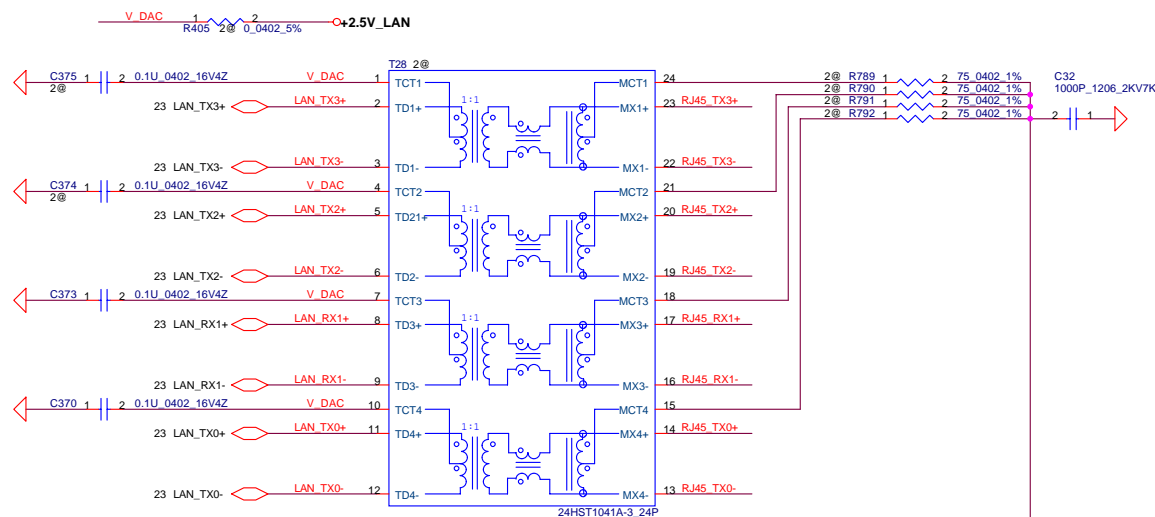
IRQ how to assign

CD-ROM Connector



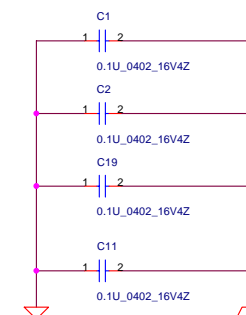
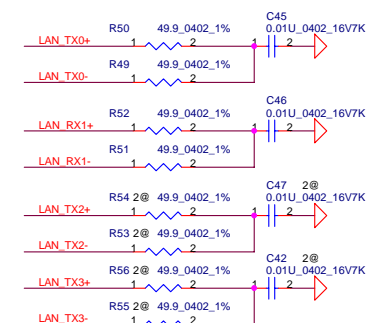
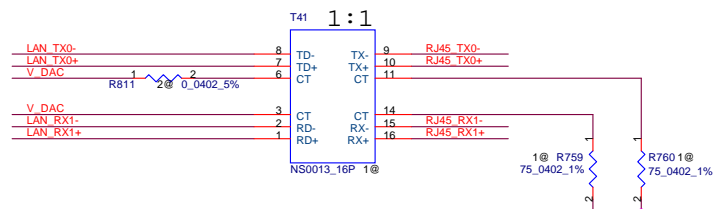
Layout Note: W=80 mils

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RTL8110SBL used the 24HST1041A-3 24P

Layout Note
24HST1041A-3 pls close to conn.



Termination plane should be copled
to chassis ground and also depends
on safety concern

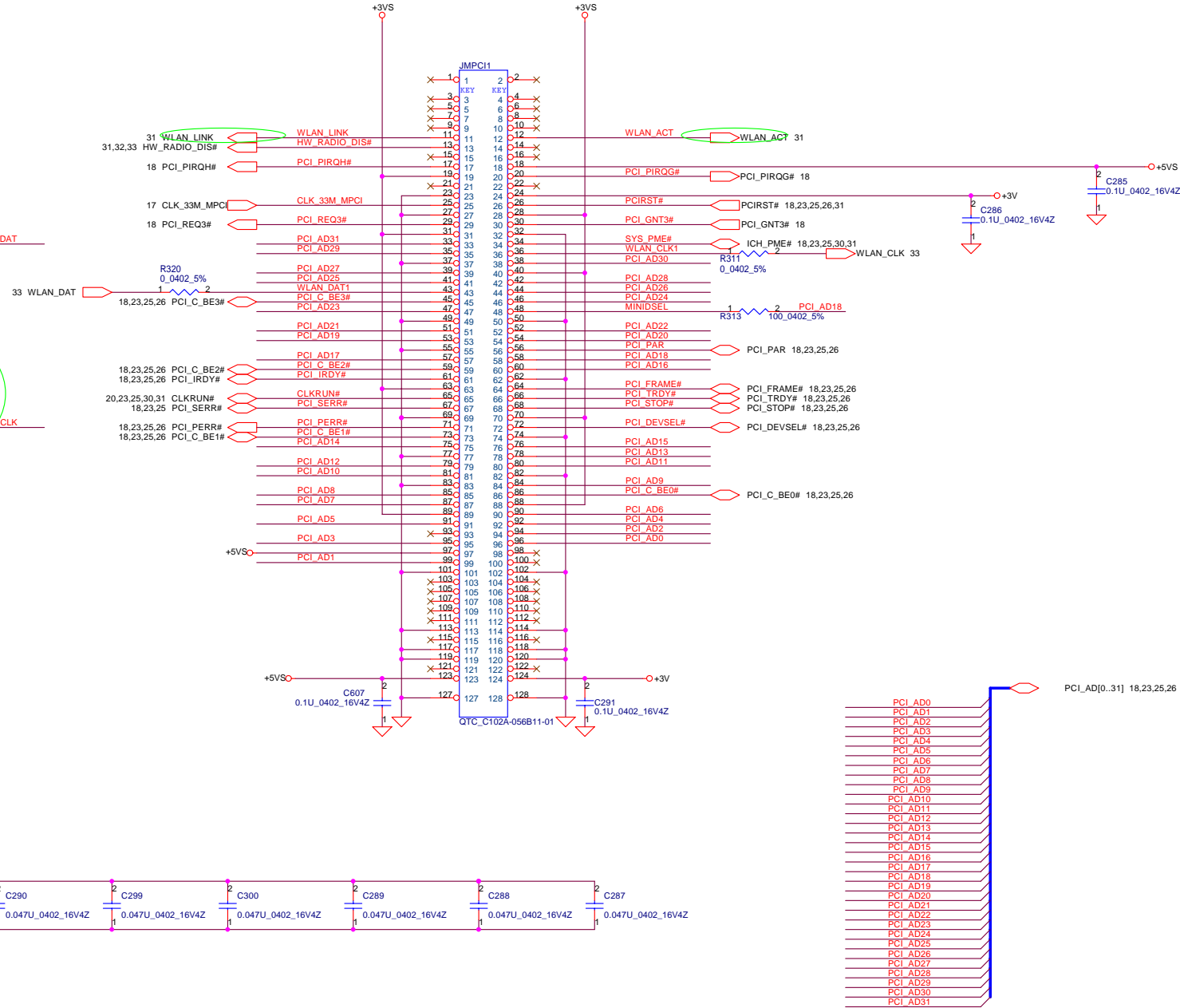
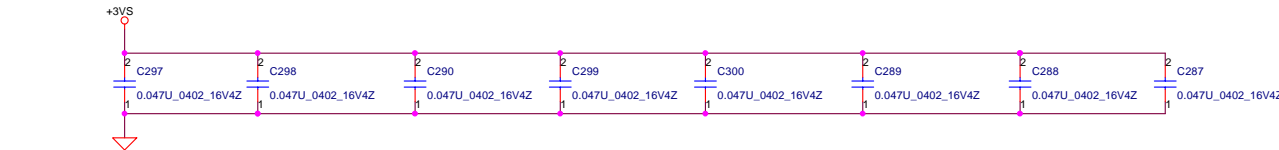
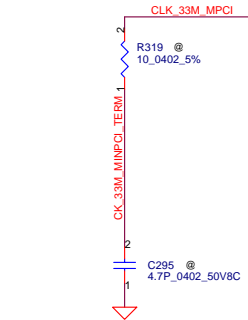
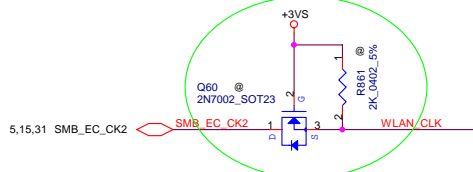
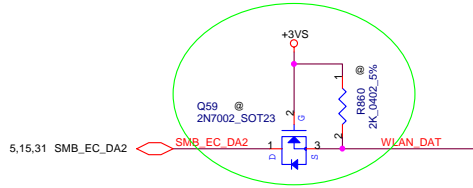
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				Size	Document Number LA-3091	1.0
Date:				Tuesday, January 10, 2006	Sheet	24 of 44



Intel WLAN HW Spec

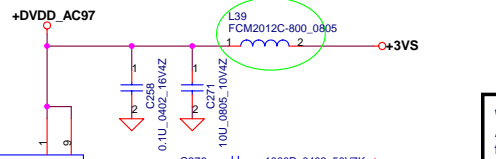
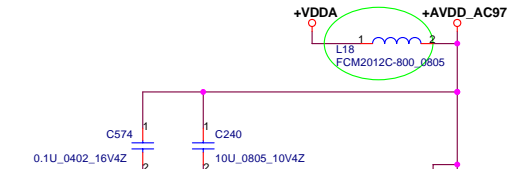
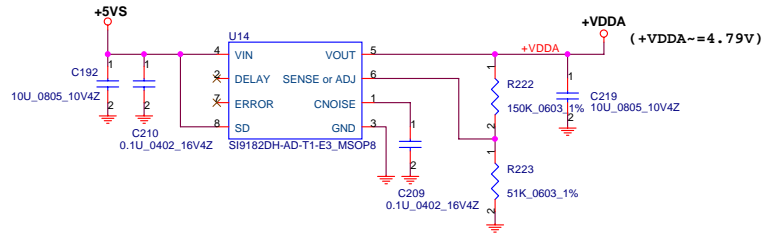
Pin36:
Channel_Clk/BT_PRIORITY

Pin43:
Channel_Data_11b_activity



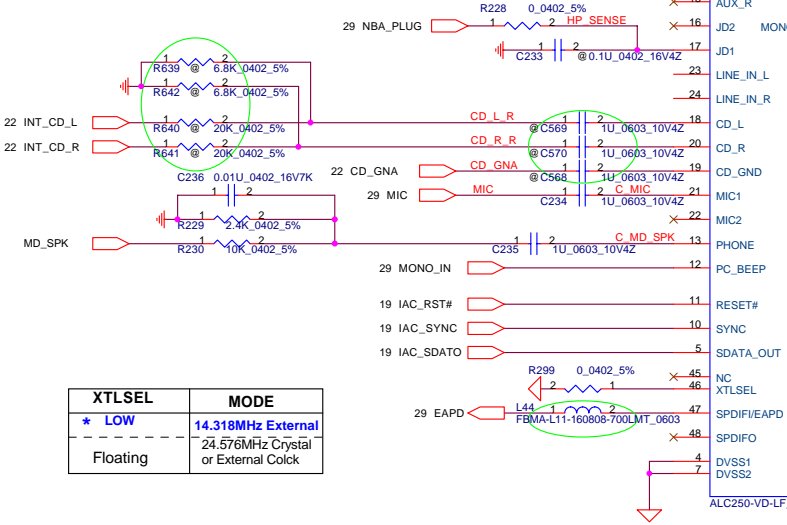
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Size	Document Number	Rev		Date	
LA-3091	1.0	Tuesday, January 10, 2006		Sheet 27 of 44	

AC97 Codec

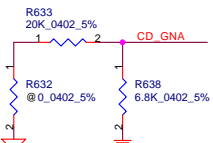


When Project need implement Headphone channel output from Audio Codec pin 39 & 41, it must have another driver to support JD function to change signal path from LINE_OUT_L & LINE_OUT_R to HP_OUT_L & HP_OUT_R when headphone insert.

For ALC250 disable HW EQ when Headphone plug-in.

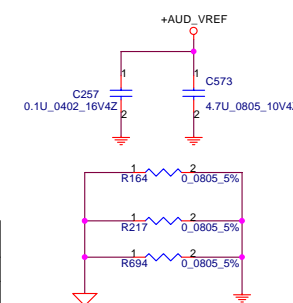


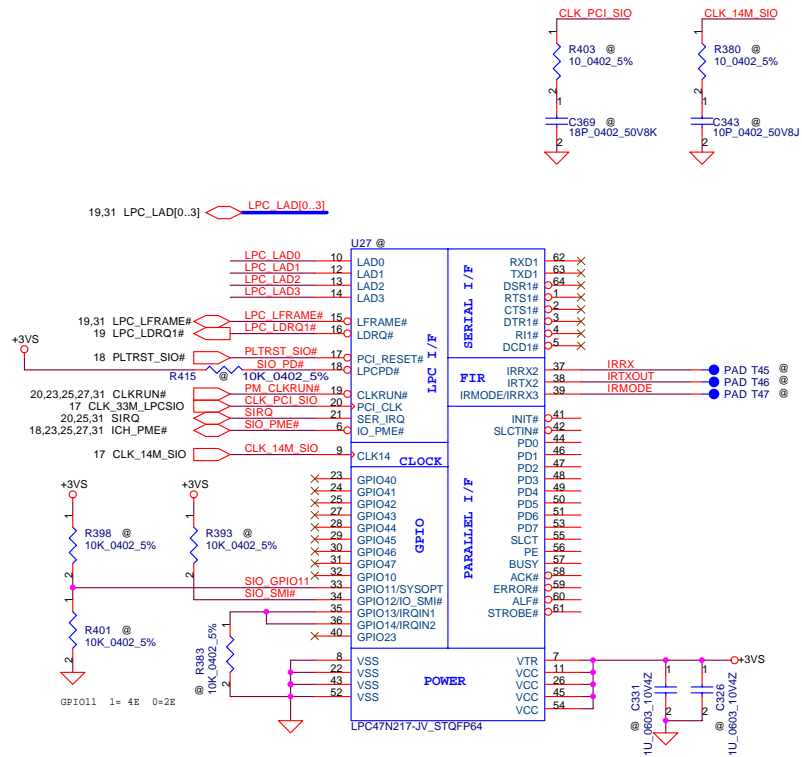
XTLSEL	MODE
★ LOW	14.318MHz External
Floating	24.576MHz Crystal or External Colck



If Project need to implement Realtek Power Off CD play function. It must be supplied power for AVDD(Pin25 & 38) & VAUX(Pin34) & power off for DVDD(Pin1 & 9). When AVDD & VAUX powered and DVDD without power, it will bypass CD L & CD_R to LINE_OUT_L & LINE_OUT_R.

MODE	SHUT DOWN	POWER OFF CD Play	NORMAL	NORMAL
DVDD(1/9)	0	0	1	1
VAUX(34)	0	1	0	1





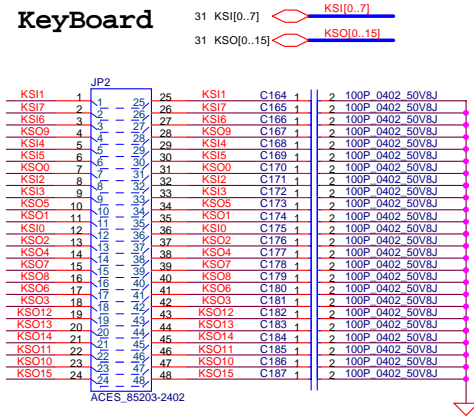
FIR Module

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				Size	Rev
Date: Tuesday, January 10, 2006				Sheet 30 of 44	1.0

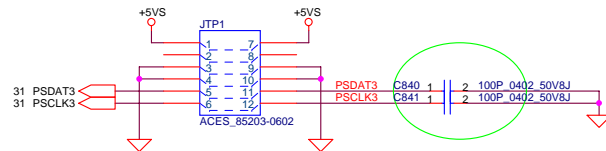


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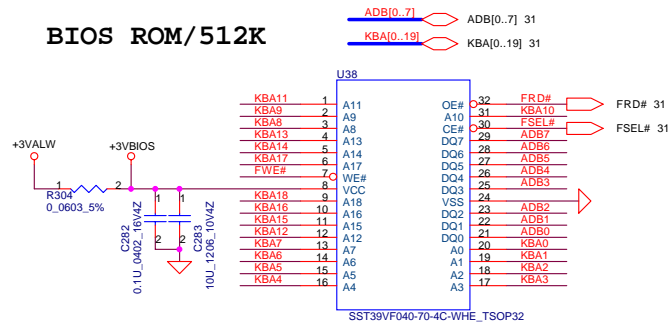
KeyBoard



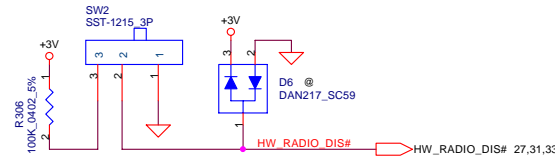
T/P



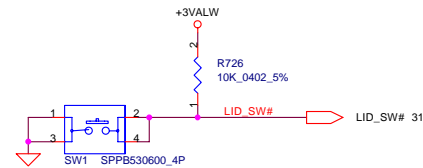
BIOS ROM/512K



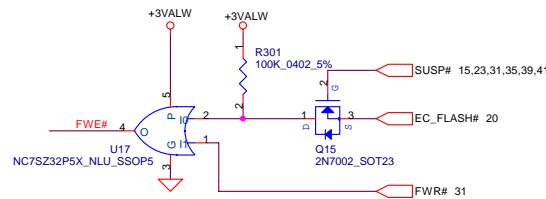
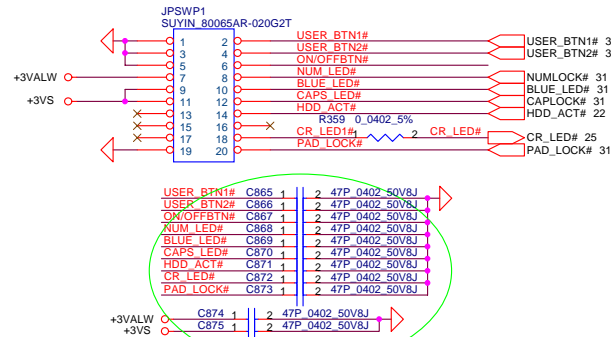
Killer switch



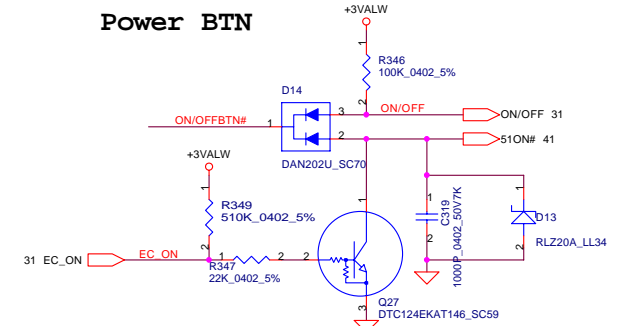
LID Switch



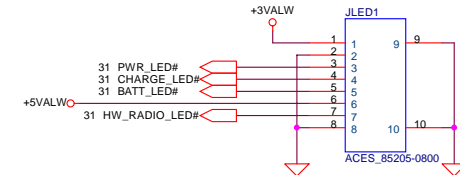
SW Board



Power BTN

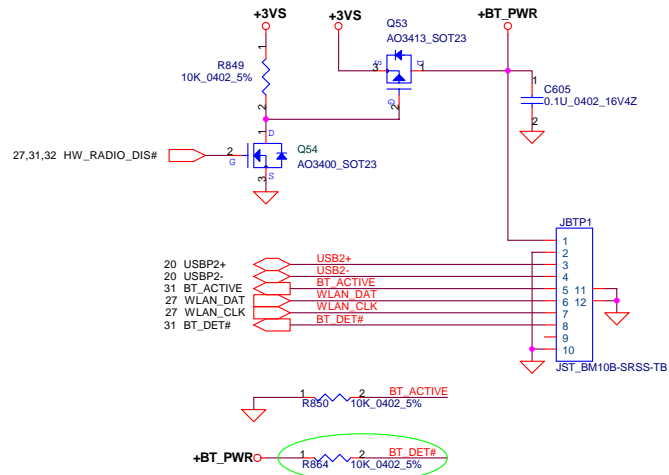


LED Board

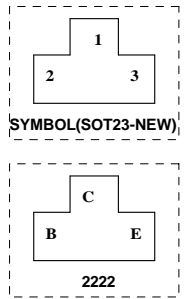
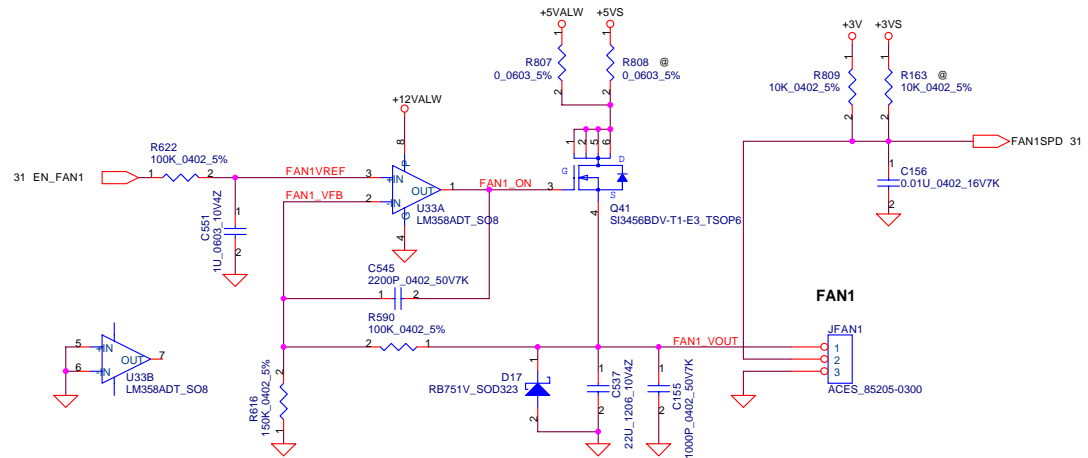


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						Size		Document Number		1.0	
						Date:		Tuesday, January 10, 2006		Sheet 32 of 44	

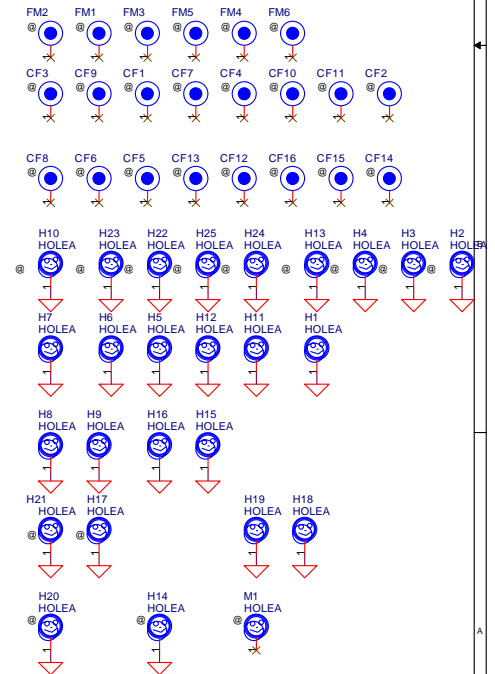
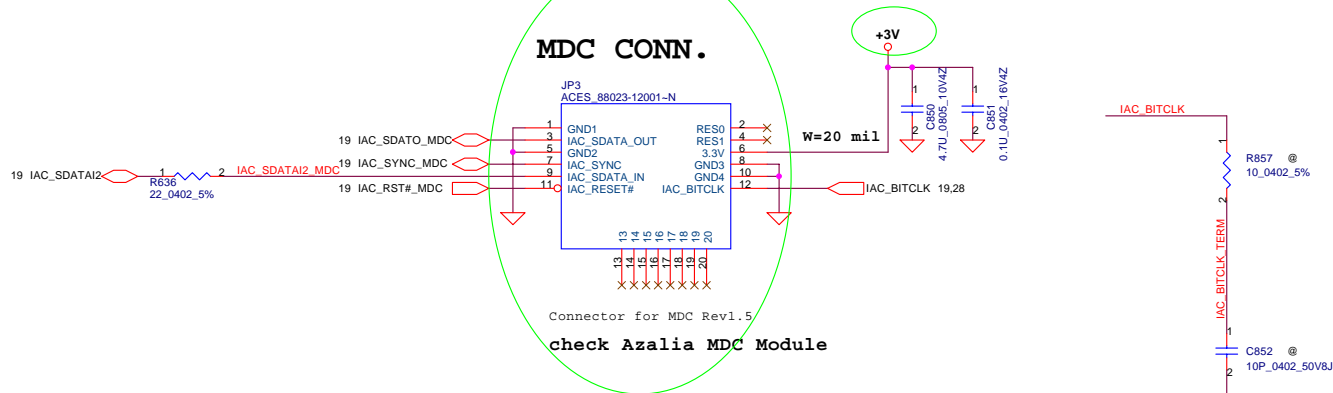
Blue Tooth



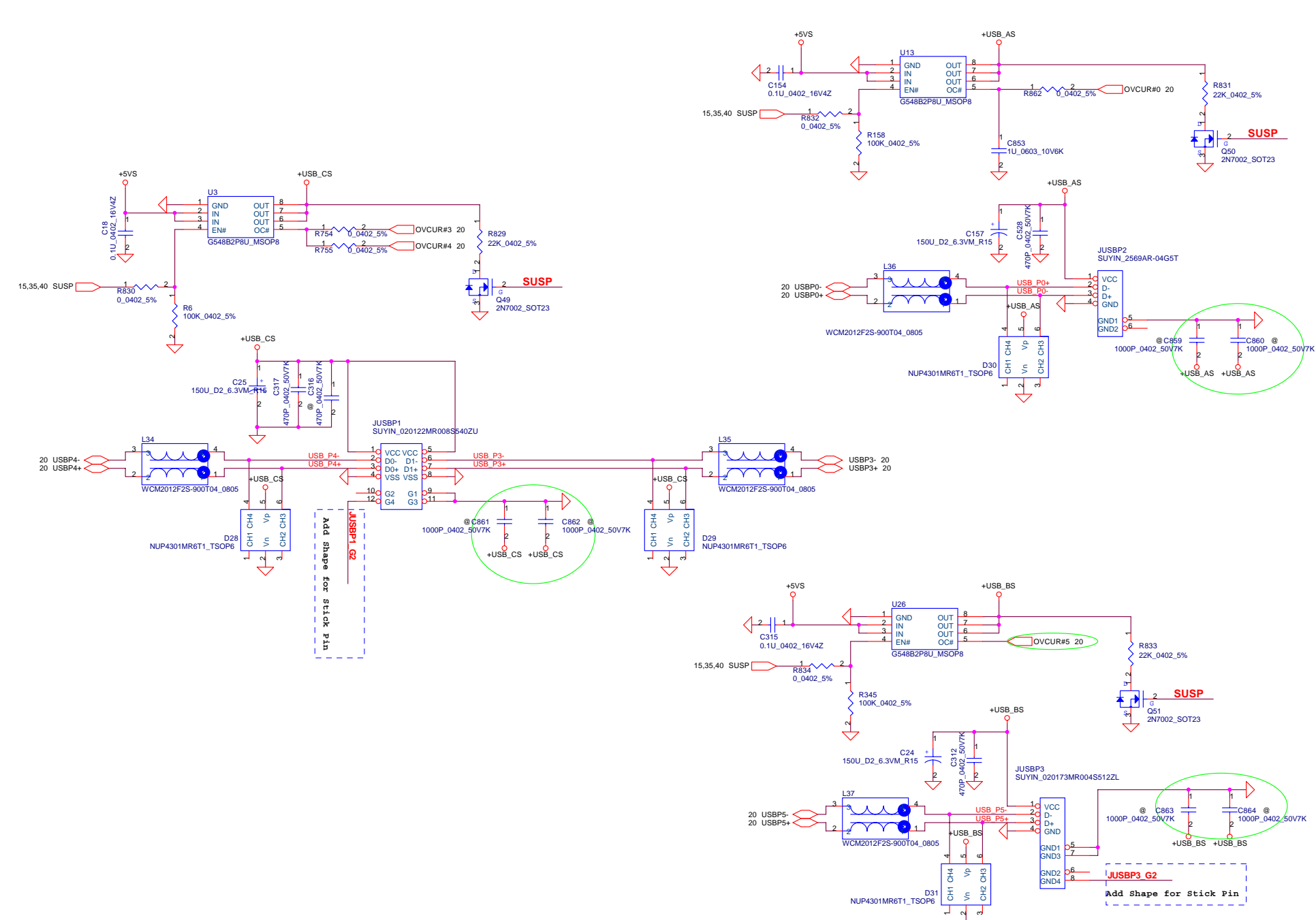
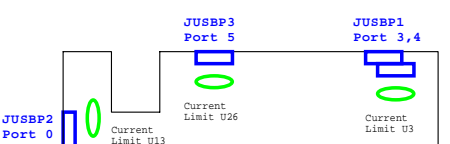
FAN1 Control and Tachometer



MDC CONN.

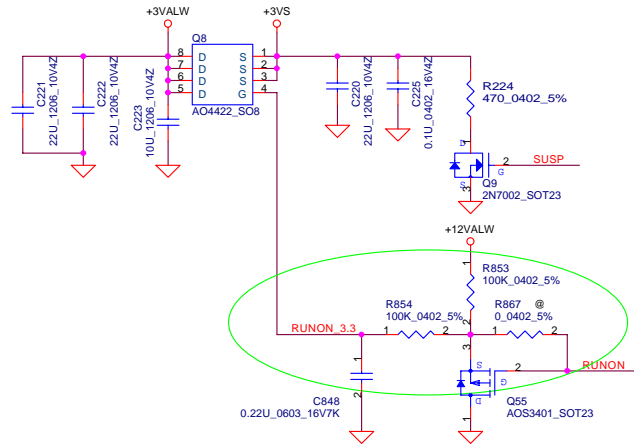


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				CustomLA-3091	1.0
				Date: Tuesday, January 10, 2006	Sheet 33 of 44

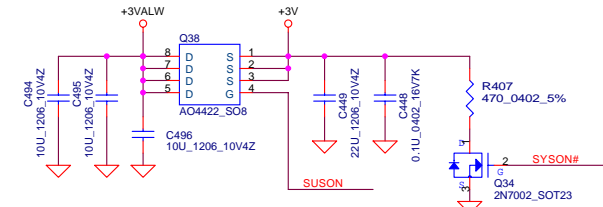


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Size		Document Number		Rev	
Date:		Tuesday, January 10, 2006		Sheet 34 of 44	

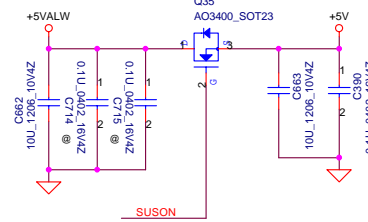
+3VALW to +3VS Transfer



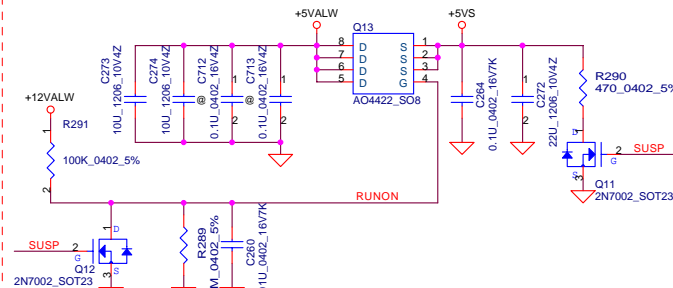
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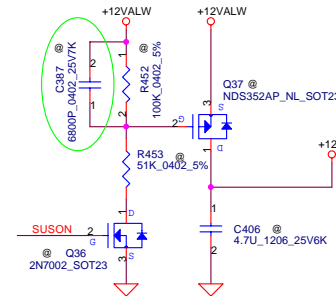
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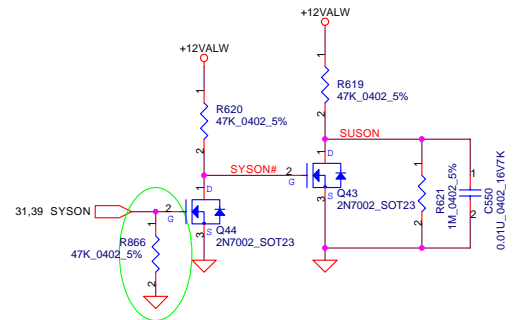
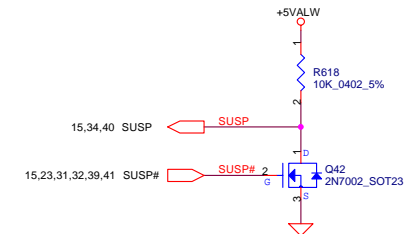
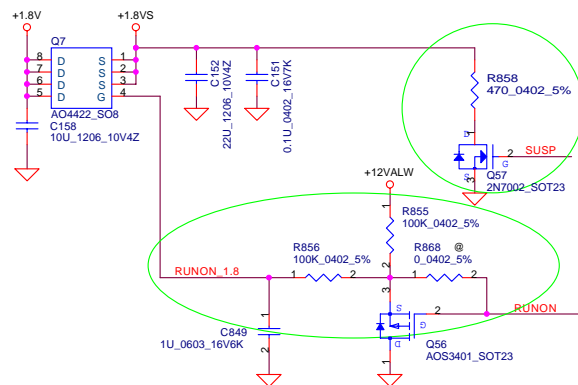
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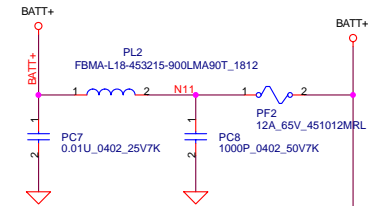
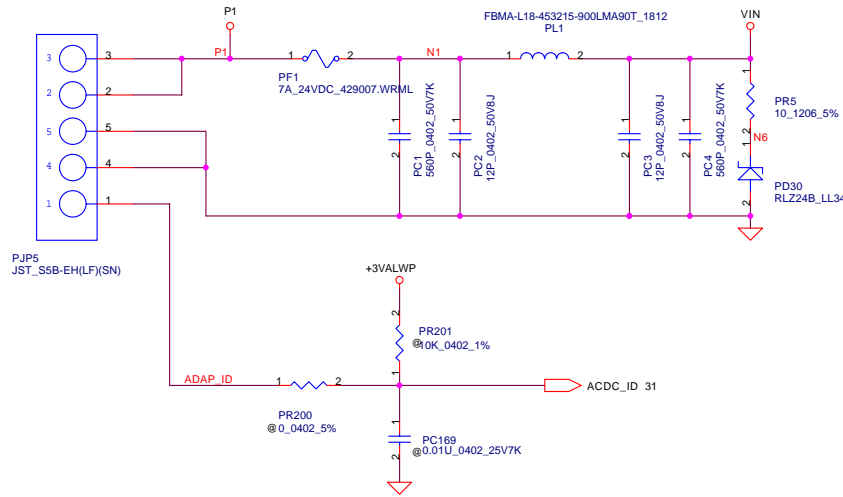
+12VALW to +12V Transfer



+1.8V to +1.8VS Transfer

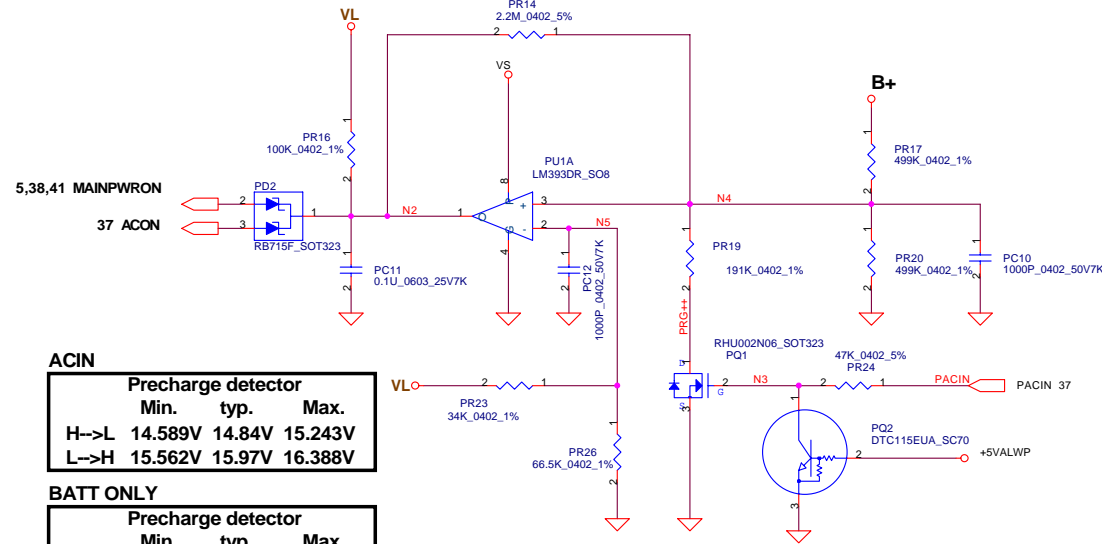


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PJPB1 battery connector

SMART Battery:
1.BAT+
2.ID
3.B/I
4.TS
5.SMD
6.SMC
7.GND

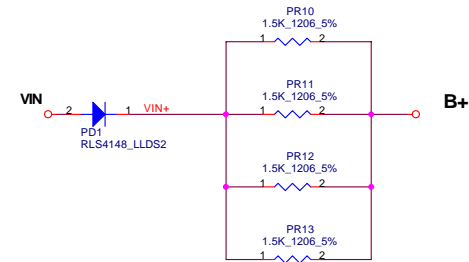


ACIN

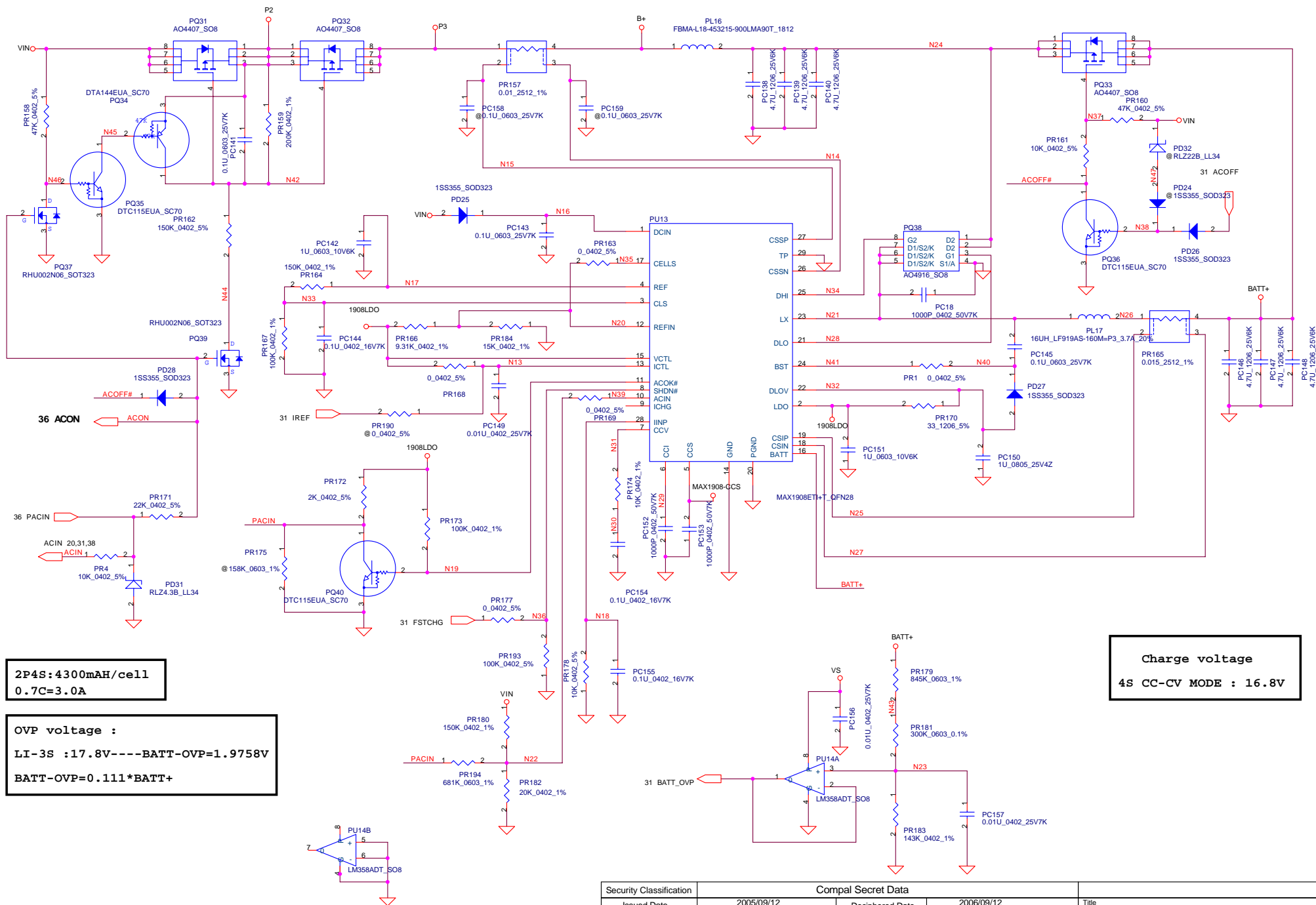
Precharge detector			
Min.	typ.	Max.	
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

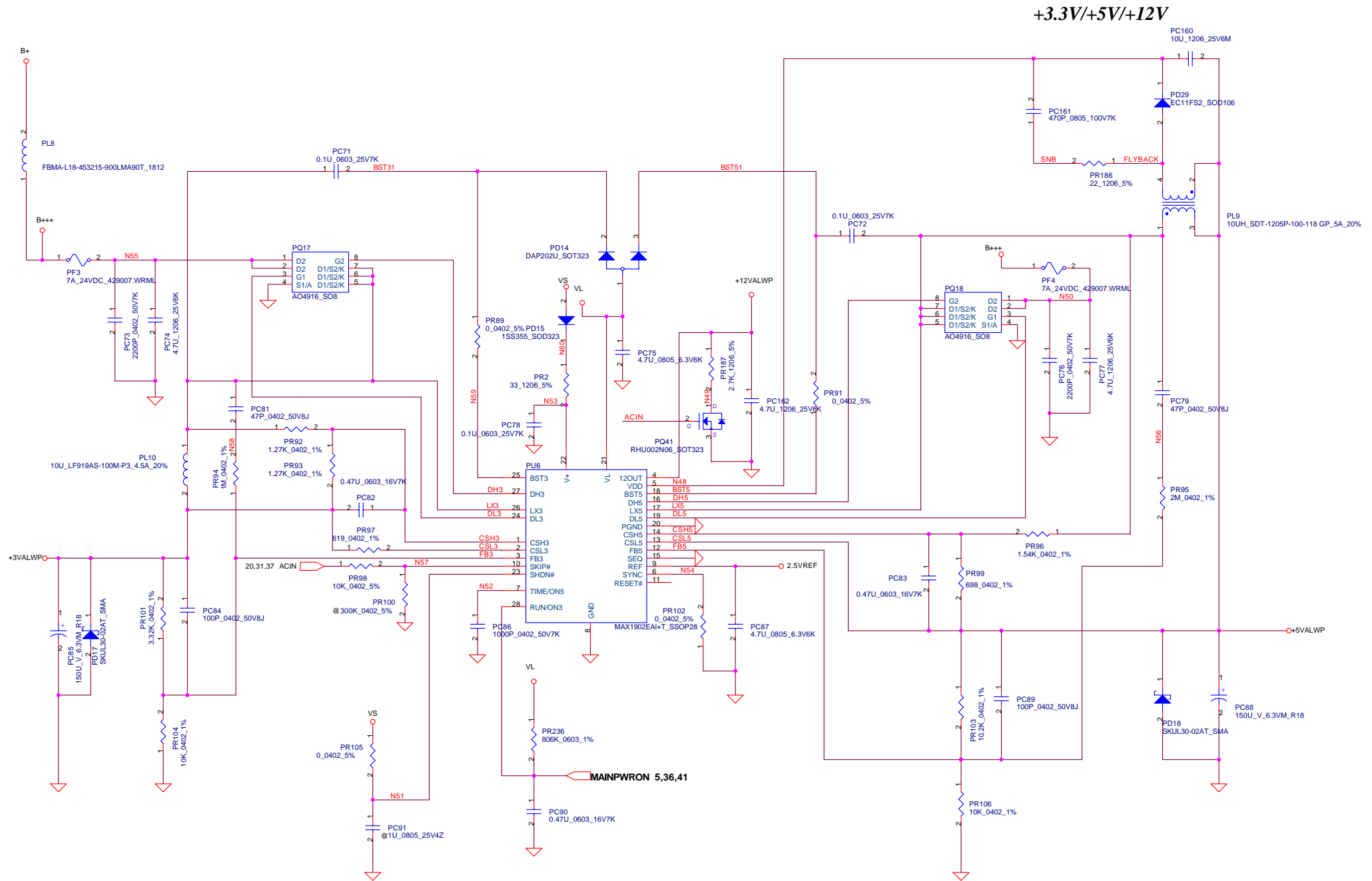
BATT ONLY

Precharge detector			
Min.	typ.	Max.	
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



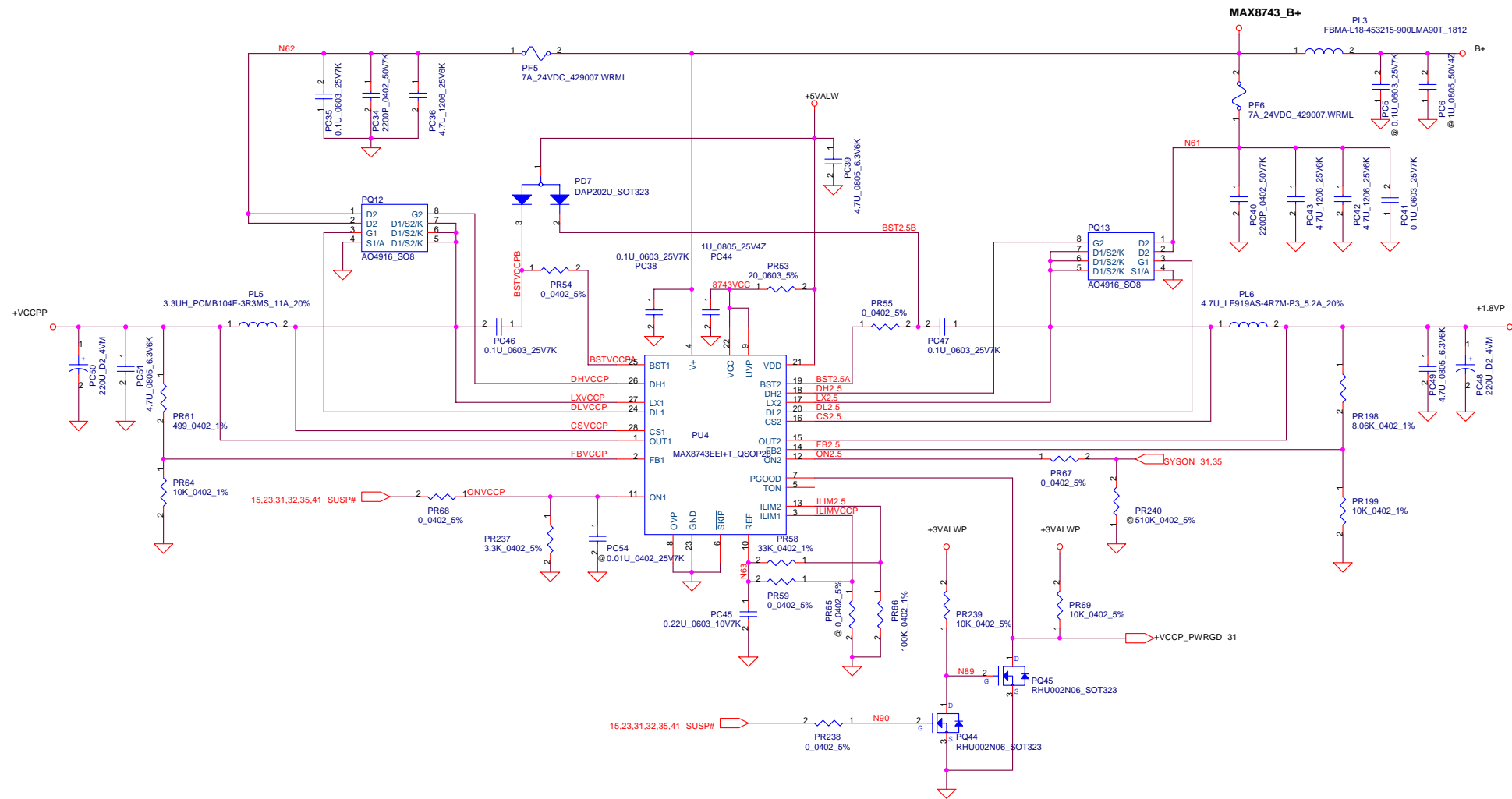
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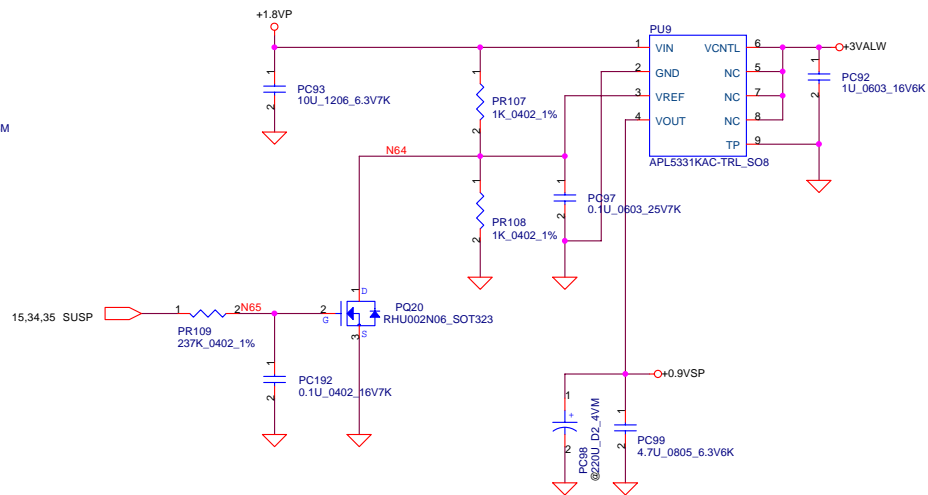
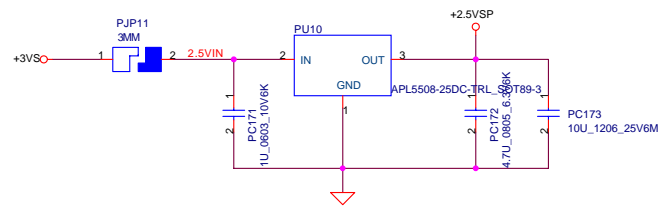
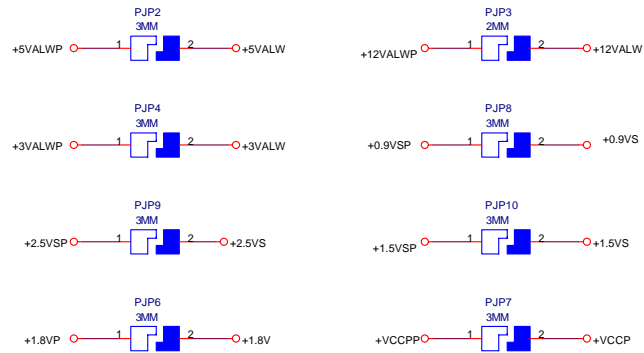
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+1.8VP / +VCCPP



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				Date:	Tuesday, January 10, 2006	Sheet 39 of 44

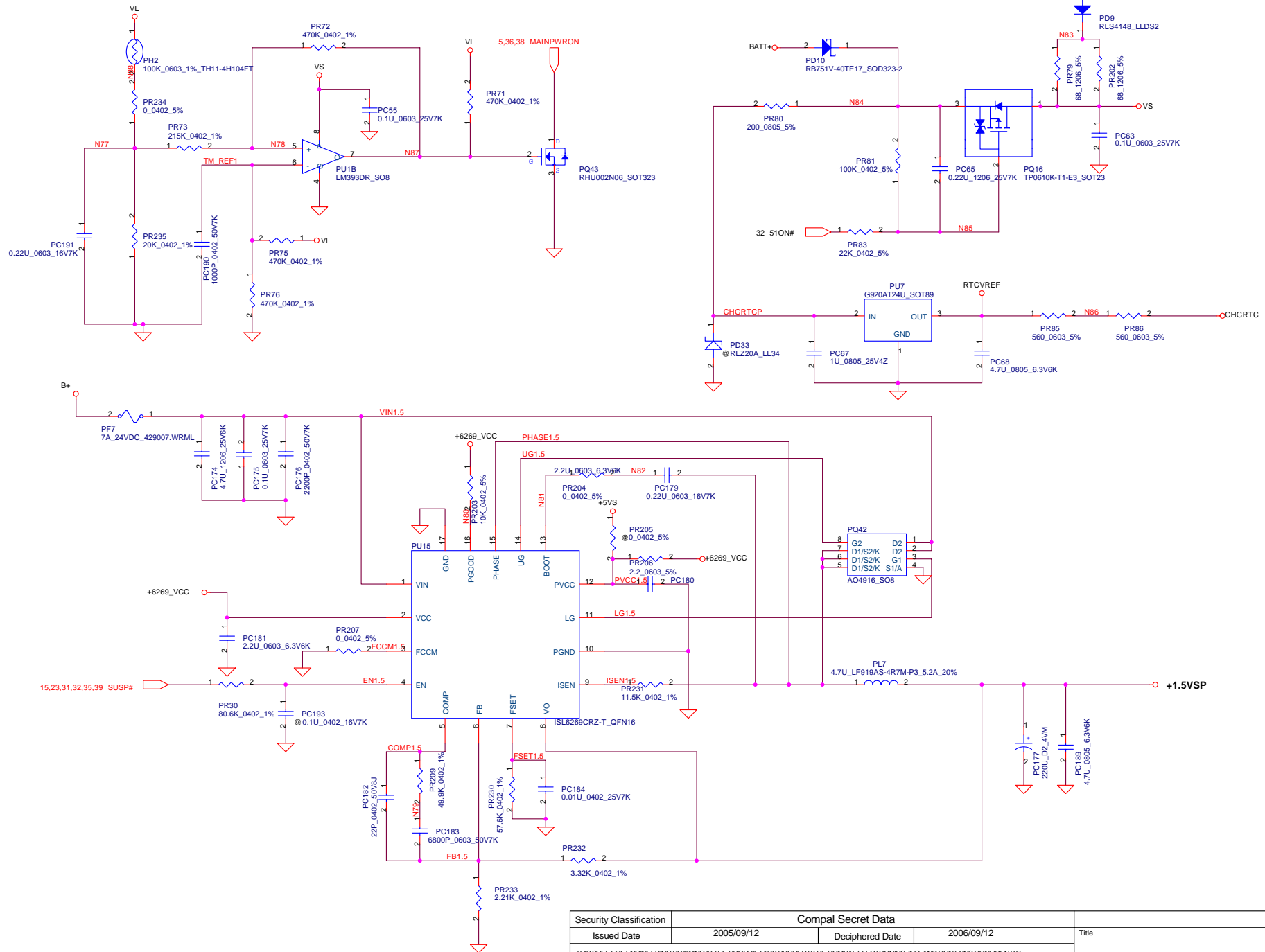
+0.9VSP / +2.5VSP



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				Date:	Tuesday, January 10, 2006
				Sheet	40 of 44

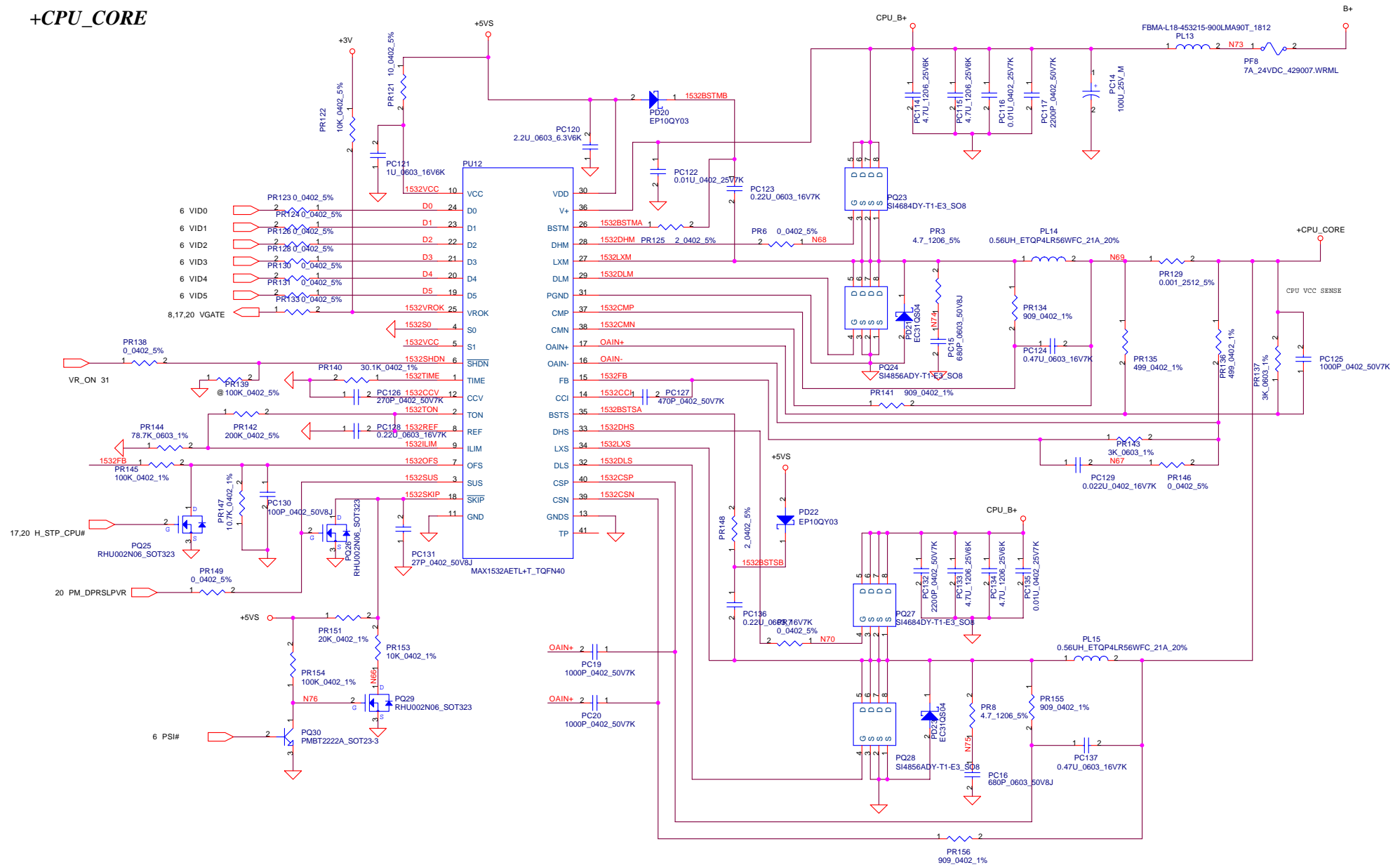
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

RTC Battery & OTP & +1.5VSP



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+CPU_CORE



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Version change list (P.I.R. List)

Item	Reason for change	Modify List	PG#	Rev.	Phase
1	Solve NB thermal issue	Add C855 S CER CAP 4.7U 6.3V K X5R 0805 Change C393 to S CER CAP 4.7U 6.3V K X5R 0805	11	0.2	EVT to DVT
2	Avoid +LCDVDD voltage transfer loss from +3.3V to +3.1V	Change Q26 to S TR SI4410DY-T1-A 1N SO-8	15		
3	Avoid can't turn on LCD	Change U1 to S IC NC7SZ08P5X_NL SC70 5P AND Add Q58 S TR BSS138LT1G 1N SOT23 W/D Add R859 S RES 1/16W 4.7K +-5% 0402	15		
4	Fix R G B rising time fail	Change L3,L4,L5 to S SUPPRE_ TAI-TECH FCM2012CF-800T06 0805	16		
5	Common Clock Generator Design	Change U31 to S IC IC954226AGLFT TSSOP 56P CLK GEN	17		
6	Correct can't power on when adapter plug-in	Remove Q47 S TR 2N7002 1N SOT-23 only for BOM	20		
7	Avoid TP short when plug-in	Delete JTP1 pin2 net from +5VS	32		
8	Fine tune +3VS power sequence	Add R853,R854 S RES 1/16W 100K +-5% 0402 C848 S CER CAP .22U 16V K X7R 0603 Q55 S TR AO3401L 1P SOT23	36		
9	Fine tune +1.8VS power sequence	Add R855,R856 S RES 1/16W 100K +-5% 0402 C849 S CER CAP 1U 16V K X5R 0603 TAIYO Q56 S TR AO3401L 1P SOT23	36		
10	Add +1.8VS dis-charge circuit	Add R858 S RES 1/16W 470 +-5% 0402 Q57 S TR 2N7002 1N SOT-23	36		
11	Change MDC module from V1.0 to V1.5	Change JP3 from S H-CONN ACES 88021-30011 30P P0.8 to S H-CONN FOXCON QT8A0121-6011-8F 12P P.8	34		
12	Change NB L material to reduce Voltage lose	Change L11,L19,L20L23 from S SUPPRE_ CHENG-HANN MBK1608301YZF 0603 to S SUPPRE_ KC FBMA-L11-160808-700LMT 0603	11	0.3	DVT to PVT & SVT
13	Reduce USB over current signal nosie	Add C856,C858 S CER CAP 1U 10V K X5R 0603	20		
14	Fix ODD can't detect issue	Remove Q17,Q14 only fro BOM and delete D27,R813 Add R813 S RES 1/16W 0 +-5% 0402	22		
15	Eliminate LAN ISOLATE# voltage leakage	Add Q61 S TR AO3413 1P SOT23-3 R43 S RES 1/16W 1K +-1% 0402 R46 S RES 1/16W 15K +-1% 0402	23		
16	Fix MS/SD can't detect issue	Remove R454,R468,R495,R463,R500,R505,R439 S RES 1/16W 43K +-5% 0402 fro SD Remove R432,R419,R402,R414,R431 S RES 1/16W 43K +-5% 0402 for MS Delete U30 pin9 link to +12V	25		
17	Fix SPK niose issue	Remove R639,R642,R640,R641,C569,C568,C570 Change R851 to L44 S SUPPRE_ KC FBMA-L11-160808-700LMT 0603 Change L18,L39 to S SUPPRE_ TAI-TECH FCM2012CF-800T06 0805 Change R285 to L44 S SUPPRE_ KC FBMA-L11-160808-700LMT 0603	28		
18	Fix SPK niose issue	Add C162,C161,C160,C159 S CER CAP 22P 25V K NPO 0402 Add L45,L46 S SUPPRE_ KC FBMA-L11-160808-700LMT 0603 Deletet C844 S CER CAP 220P 50V K X7R 0402 Change L29 to S RES 1/10W 0 +-5% 0603	29		
19	Fix MDC can't wake up on ring issue	Change JP3 pin6 link to +3V	33		
20	Delete USB Conn	Delete JUSBP4,D32,L38,C839	34		
21	Eliminate SYSON voltage surge issue	Add R866 S RES 1/16W 47K +-5% 0402	35		
22	Fix USB can't detect issue	Delete L40,L41,L42	34	1.0	SVT to MP v2.0
23	Avoid CRT voltage leakage to +5VS	Change R321 and R325 link to +CRT_VCC (original link to +5VS)	16		MP v2.0 to MP v3.0

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Version change list (P.I.R. List)

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Item	Reason for change	Modify List	PG#		B.Ver#	Phase
1	Adjust 0.9VSP power sequence	Add PR109 237K_0402_1% and PC192 0.1U_0402_16V delay 0.9VSP.	41	2005.10.23		
2	Adjust 1.5VSP power sequence	Add PR30 80.6K_0402_1% and PC193 0.1U_0402_16V delay 1.5VSP.	42	2005.10.23		
3	Improve 1.8VP, VCCP, 1.5VSP transient response	Change PC50, PC48, PC177 from 150u 6.3v to 220u 4v	40 B42	2005.10.23		
4	To solve susp# leakage from +3valwp	Delete PD3	39	2005.12.01		
5	To avoid +VCC_PWRGD trun on beofre +VCCP turn on.	Add PQ44, PQ45 RHU002N06_SOT323, PR238 0_0402_5%, PR239 10K_0402_5%	39	2005.12.01		
6	Adjust 1.5v back to A-test status.	Delete PC193 at BOM.	41 B42	2005.12.01		
7						
8						
9						
10						
11						
12						
13						

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